10/602,292 EIC SEARCH 08/03/2007

Patent Abstracts

File 347:JAPIO Dec 1976-2007/Dec(Updated 070702)
(c) 2007 JPO & JAPIO
File 350:Derwent WPIX 1963-2007/UD=200749
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Set	Items	Description
S1	17254	MULTIPROCESSOR??? OR MULTI???()PROCESSOR???
S2	3658350	IMPORT?? OR IMPORTING OR EXPORT??? OR SEND??? OR TRANSFER? ? OR TRANSFERR??? OR COPY??? OR TRANSMIT? OR TRANSMISSION? ? - OR DISPATCH???
S3	48532	S2(3N)(SUSPEND? OR STALL??? OR DISCONTINU??? OR DELAY??? OR POSTPON??? OR DEFER??? OR INTERRUPT??? OR ABANDON?? OR HALT?-?? OR TERMINAT??? OR CEASE? ? OR CEASING OR DISRUPT???)
S4	3601735	DATA OR INFO OR INFORMATION OR MESSAGE? OR REPORT?
S5	51424	S4(3N)(SUSPEND? OR STALL??? OR DISCONTINU??? OR DELAY??? OR POSTPON??? OR DEFER??? OR INTERRUPT??? OR ABANDON?? OR HALT?-?? OR TERMINAT??? OR CEASE? ? OR CEASING OR DISRUPT???)
S6	3084323	BUFFER? OR CACHE? OR MEMORY OR STOR?
S7	2295	S5(5N)(PRIOR OR BEFORE???? OR PREVIOUS? OR PROCED??? OR IN-ITIAL? OR EARLY OR EARLIER)
S8	2752	S3(5N)(AFTER???? OR LATER OR FOLLOW??? OR NEXT)
S9	3	S1 AND S7 AND S8
S10	2	S9 NOT AY=2002:2007
S11	339	S1 AND S3 AND S4
S12	226	S11 AND S6
S13	30	S1(25N)S3(25N)S5
S14	15	S13 AND S6
S15	15	S14 NOT AY=2002:2007
S16	15	S15 NOT S10
S17	11844	S1 AND S6
S18	44	S17 AND (S7 OR S8)
S19	23	S17(25N)(S7 OR S8)
S20	2	S9 NOT AY=2002:2007
S21	0	S20 NOT (S16 OR S10)

10/3,K/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0009090610 - Drawing available
WPI ACC NO: 1999-009222/199901
XRPX Acc No: N1999-006694
Controlling method of communication of digital message among host and auxiliary processing units - involves transmitting message interrupt identifying atleast one data message to be processed, from one hpu and apu to other only after reception of token interrupt
Patent Assignee: LUCENT TECHNOLOGIES INC (LUCE)
Inventor: CHANG L F; HEWETT A P W; ROUSE D M
Patent Family (1 patents, 1 countries)

Patent			Application			
Number	Kind	Date	Number	Kind	Date	Update
US 5835779	A	19981110	US 1996617947	A	19960315	199901 B

Priority Applications (no., kind, date): US 1996617947 A 19960315

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 5835779	A	EN	8	5	

Original Publication Data by Authority

Original Abstracts:
The transmission of messages among **multiple processors** is controlled by **the** use of token and message interrupts. A token interrupt must be received from the processor...

...demands, i.e. sending a message interrupt, to the processor. Message interrupts, which may only **be transmitted following** receipt of **a token interrupt**, identify commands and user messages to be processed by a receiving processor. This permits instructions...
Claims:
...the one processing unit must be given before the other processing unit is permitted to **transmit a message interrupt** to the one processing unit.

10/3,K/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0006315777 - Drawing available
WPI ACC NO: 1993-111083/199314
XRPX Acc No: N1993-084599
Dual bus structure computer data transfer management - allowing Alternate Bus Master unlimited use of system bus master memory when in possession of card to card communication bus
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: ENG R C; GALELLA J W; MCCARARY R E; MCCRARY R E; MCDONALD M G;

STELZER E H; YENTZ F C

Patent Family (7 patents, 4 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
EP 535793	A2	19930407	EP 1992307290	A	19920810	199314 B
CA 2068010	A	19930301	CA 2068010	A	19920505	199320 E
EP 535793	A3	19930714	EP 1992307290	A	19920810	199406 E
US 5469577	A	19951121	US 1991752725	A	19910830	199601 E
			US 1994250328	A	19940527	
CA 2068010	C	19961022	CA 2068010	A	19920505	199702 E
EP 535793	B1	19970521	EP 1992307290	A	19920810	199725 E
DE 69219848	E	19970626	DE 69219848	A	19920810	199731 E
			EP 1992307290	A	19920810	

Priority Applications (no., kind, date): US 1994250328 A 19940527; US 1991752725 A 19910830

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
EP 535793	A2	EN	19	6	
Regional Designated States,Original: DE FR GB IT					
CA 2068010	A	EN			
EP 535793	A3	EN			
US 5469577	A	EN	18	6	Continuation of application US 1991752725
CA 2068010	C	EN			
EP 535793	B1	EN	18	6	
Regional Designated States,Original: DE FR GB IT					
DE 69219848	E	DE			Application EP 1992307290
					Based on OPI patent EP 535793

Original Publication Data by Authority

Original Abstracts:

...transfers. The invention promptly services pending memory refresh requests; limits multiple accesses to on card (**or processor** complex) memory by an Alternate Bus Master to a predetermined number of cycles where the...

Claims:

...when a said first priority condition is first detected during said given cycle, and said **suspending** step **is** applied **after** a predetermined number of n cycles (n>1) of said data transfer activity following said...

...respective access of said ABMB device to said local bus; and wherein: when said cycles **of data** transfer activity by **said** ABMB device are suspended due to detection of a said first priority condition during a...

...of data transfer activity which resume after the suspension ends; and when said cycles of **data transfer** activity are **suspended** due to detection of a said second priority condition in said given cycle, performance of a single instance **of** said handshake **procedure is** distributed over all cycles of data transfer activity preceding the suspension, including said given cycle...

16/3,K/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO
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04812431
METHOD AND APPARATUS FOR **TRANSFER** OF **INTERRUPT INFORMATION** AT INSIDE OF **MULTIPROCESSOR** COMPUTER SYSTEM

PUB. NO.: 07-105031 [JP 7105031 A]
PUBLISHED: April 21, 1995 (19950421)
INVENTOR(s): RONARUDO SABUIERU AROYO
UIRIAMU BURENTO CHIYANDORAA
JIYOOJI UIRIAMU DARII JIYUNIA
APPLICANT(s): INTERNATL BUSINESS MACH CORP <IBM> [000709] (A Non-Japanese Company or Corporation), US (United States of America)
APPL. NO.: 06-187212 [JP 94187212]
FILED: August 09, 1994 (19940809)
PRIORITY: 7-124,513 [US 124513-1993], US (United States of America), September 20, 1993 (19930920)

METHOD AND APPARATUS FOR **TRANSFER** OF **INTERRUPT INFORMATION** AT INSIDE OF **MULTIPROCESSOR** COMPUTER SYSTEM
...JAPIO CLASS: **Memory** Units); 45.4 (INFORMATION PROCESSING

16/3,K/2 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO
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03111757 **Image available**
DATA PROCESSOR

PUB. NO.: 02-087257 [JP 2087257 A]
PUBLISHED: March 28, 1990 (19900328)
INVENTOR(s): SANO RYOICHI
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 63-238740 [JP 88238740]
FILED: September 26, 1988 (19880926)
JOURNAL: Section: P, Section No. 1065, Vol. 14, No. 289, Pg. 26, June 21, 1990 (19900621)

ABSTRACT
PURPOSE: To improve data transfer efficiency by providing the data **buffer** of a first in first out (FIFO) system which is connected to an external data...

...informed in correspondence to the contents of the status register 5 that there is the **transferring** of **data interruption** to the external processor or the exterminal and internal processors. Accordingly, when the data are transferred between two **multi - processors** which are mutually connected, it is not necessary to once house the data in an...

16/3,K/3 (Item 1 from file: 350)

DIALOG(R)File 350:Derwent WPIX

0015627847 - Drawing available
WPI ACC NO: 2006-192024/200620
Related WPI Acc No: 2007-100079
XRPX Acc No: N2006-165367
Method of reducing information reception delays for voice over internet protocol application, involves sending original message and copies of original message through connections established between sender and recipient computing devices
Patent Assignee: MICROSOFT CORP (MICT)
Inventor: HAN M; VEGA G A; VEGA GARCIA A; ZHONG W
Patent Family (2 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
US 20060041698	A1	20060223	US 2004856254	A	20040527	200620 B
US 7080173	B2	20060718	US 2004856254	A	20040527	200648 E

Priority Applications (no., kind, date): US 2004856254 A 20040527

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 20060041698	A1	EN	12	6	

Alerting Abstract ...System for reducing information reception delay; and computer readable medium **storing** instructions for reducing information reception delay...

...USE - For reducing **information** reception **delay** using **transmission** control protocol (TCP), during exchanging of messages between server and client such as personal computer (PC), hand-held computer, **multiprocessor** system, microprocessor-based system, programmable consumer electronics, network PC, minicomputer, mainframe computer, laptop device e...

Original Publication Data by Authority

Claims:
...created connection, the redundant copy of the original messages containing key frames and delta frames; **storing** the received delta frames;when a message containing a key frame is not received within...

16/3,K/4 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0015115891 - Drawing available
WPI ACC NO: 2005-465382/200547
XRPX Acc No: N2005-377746
Interrupts dispatch **method in multi-** processor **system, involves identifying target processor from** multiple processors **, based on interrupt weighted average of processors calculated from their respective** interrupt dispatch information
Patent Assignee: EDIRISOORIYA S J (EDIR-I); JAMIL S (JAMI-I); MINER D E (MINE-I); NGUYEN H T (NGUY-I); OBLENESS R F (OBLE-I); TU S J (TUSJ-I);

INTEL CORP (ITLC)
Inventor: EDIRISOORIYA S J; JAMIL S; MINER D E; NGUYEN H T; OBLENESS R F; TU S J
Patent Family (2 patents, 2 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
US 20050125582	A1	20050609	US 2003730467	A	20031208	200547 B
CN 1737765	A	20060222	CN 200410010458	A	20041208	200639 E

Priority Applications (no., kind, date): US 2003730467 A 20031208

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 20050125582	A1	EN	11	4	

Interrupts dispatch **method in multi-** processor **system, involves identifying target processor from** multiple processors **, based on interrupt weighted average of processors calculated from their respective** interrupt dispatch information

Alerting Abstract ...NOVELTY - An interrupt weighted average (IWA) is generated for each of the **multiple processors** , based on the **interrupt dispatch information** associated with the processors. A target processor is identified from the **multiple processors** , based on the IWAs, for **dispatching** an **interrupt** . ...machine readable medium **storing** instruction for dispatching interrupts; interrupts dispatch apparatus; and multi-processor system...

Original Publication Data by Authority

Original Abstracts:
Methods and apparatus to **dispatch interrupt** requests in **multi-processor** systems are disclosed. In an example method, an interrupt weighted average (IWA) of each of a plurality of processors is generated based on **interrupt dispatch information** associated with the plurality of processors. Based on the IWA of each of the plurality of processors, a target processor from the plurality of processors is identified to **dispatch** an **interrupt.** >

16/3,K/5 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0013567966 - Drawing available
WPI ACC NO: 2003-662294/200362
XRPX Acc No: N2003-528558
Multiprocessor **system, has interface logic connected to** memory **controller through buses, and** delays data transmitted **over buses before the data is provided to local logic at receiving end of buses**
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: ALLEN J W; MAYFIELD M J; NG A W
Patent Family (2 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update

US 20030131138 A1 20030710 US 200242103 A 20020107 200362 B
US 7171445 B2 20070130 US 200242103 A 20020107 200710 E

Priority Applications (no., kind, date): US 200242103 A 20020107

Patent Details
Number Kind Lan Pg Dwg Filing Notes
US 20030131138 A1 EN 10 3

Multiprocessor **system, has interface logic connected to** memory **controller through buses, and** delays data transmitted **over buses before the data is provided to local logic at receiving end of buses**

Alerting Abstract ...many microprocessors (102, 104, 106, 108) each having many interfacing logics (144) connected to a **memory** controller (110) through buses (112-142) for transreceiving various signals. The interfacing logic enables the...
...110 **Memory** controller...

Title Terms.../Index Terms/Additional Words: **MEMORY** ;

Original Publication Data by Authority

Original Abstracts:
An interfacing logic is implemented in one or more processors and a **memory** controller in a **multiprocessor** system. The interfacing logic enables all processors to receive snoops and snoop responses substantially at the same time by **delaying data transmitted** over faster busses before the data is provided to a local logic at a receiving...

...The interfacing logic comprises two or more paths of a multiplexer component connected to a **storage** component. The **storage** components are connected to another multiplexer component for selecting one of the two or more...

...An interfacing logic is implemented in one or more processors and a **memory** controller in a **multiprocessor** system. The interfacing logic enables all processors to receive snoops and snoop responses substantially at the same time by **delaying data transmitted** over faster busses before the data is provided to a local logic at a receiving...

...The interfacing logic comprises two or more paths of a multiplexer component connected to a **storage** component. The **storage** components are connected to another multiplexer component for selecting one of the two or more...
Claims:
...a first interfacing logic, the first microprocessor being clocked by a first system clock;a **memory** controller connected to the first interfacing logic through at least a first bus for transmitting at least a first signal from the **memory** controller to the first interfacing logic, the **memory** controller being clocked by a second system clock; anda second microprocessor connected to the **memory** controller through at least a second bus for transmitting at least a second signal from the **memory** controller to the second processor, the second bus requiring a first period of time more...

...a first interfacing logic, the first microprocessor being clocked by a first system clock;a **memory** controller connected to the first interfacing logic through at least a first bus for transmitting at least a first signal from the **memory** controller to the first interfacing logic, the **memory** controller being clocked by a second system clock; anda second microprocessor connected to the **memory** controller through at least a second bus for transmitting at least a second signal from the **memory** controller to the second processor, the second bus requiring a first period of time more...

16/3,K/6 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0010942704
WPI ACC NO: 2001-565294/200163
XRPX Acc No: N2001-420863
Method of reducing interrupt load in a multi-processor system where two processors share memory **by interrupting only when a read operation is to be performed and the** memory **is empty**
Patent Assignee: TELEFONAKTIEBOLAGET ERICSSON L M (TELF)
Inventor: HEDMAN B; KARLSSON M
Patent Family (4 patents, 93 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
WO 2001059567	A2	20010816	WO 2001SE220	A	20010206	200163 B
AU 200132541	A	20010820	AU 200132541	A	20010206	200175 E
US 6535942	B1	20030318	US 2000500653	A	20000209	200322 E
TW 511035	A	20021121	TW 2001102226	A	20010202	200353 E

Priority Applications (no., kind, date): US 2000500653 A 20000209

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
WO 2001059567	A2	EN	13	2	

National Designated States,Original: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
Regional Designated States,Original: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW

AU 200132541	A	EN	Based on OPI patent WO 2001059567
TW 511035	A	ZH	

Method of reducing interrupt load in a multi-processor system where two processors share memory **by interrupting only when a read operation is to be performed and the** memory **is empty**
...NOVELTY - Start and end address in shared **memory** are maintained by pointers established by logic and indicate respectively where data is read from **memory** by one processor and where it is written in **memory** by the other processor. When the write pointer is equal to the read pointer, that is the **memory** is empty, and a read operation is to be performed an interrupt is generated. If...

...read and write pointers are not equal, that is there is still data in the **memory** , a further read operation is performed.
Title Terms.../Index Terms/Additional Words: **MEMORY** ;

Original Publication Data by Authority

Original Abstracts:
A method for reducing interrupt load in a **multi - processor** system is **disclosed** , **whereby** two central processors executing a real-time operating system can communicate with each other using a shared **memory** . A start pointer **and** end pointer are implemented preferably in logic. By detecting a difference in the logic values for the two pointers, the receiving CPU will receive **interrupts** only when new **data** from the **sending CPU** has arrived in the shared **memory** and the shared **memory** was empty. Consequently, **the** operating system will not be disturbed with unnecessary interruptions, and the interrupt load will thus...

...14) executing a real-time operating system can communicate with each other using a shared **memory** (16). A start pointer (18) and end pointer (**20**) are implemented preferably in logic (150). By detecting a difference in the logic values for...

...interrupts only when new data from the sending CPU (12) has arrived in the shared **memory** (16) and the shared **memory** was empty. Consequently, **the** operating system will not **be** disturbed with unnecessary interruptions, and the interrupt load will thus be low...
Claims:
...and an end pointer value, said start pointer associated with a first location in a **memory** area, and said end pointer associated with a **second** location in said **memory** area;a first processor **storing** data at said **second** location;updating said end pointer value **in** correspondence with said first processor **storing** said data at said second location;determining if said end pointer value **is** equal or not equal to said start pointer value, said start pointer value in correspondence...

16/3,K/7 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0010838706 - Drawing available
WPI ACC NO: 2001-456682/200149
Related WPI Acc No: 1999-059564
XRPX Acc No: N2001-338432
An Input/output agent method for generating interrupt request messages onto a multiprocessor system bus via the chipset includes Interrupt and destination ID corresponding with servicing processor
Patent Assignee: INTEL CORP (ITLC)
Inventor: AZIMI M; JAYAKUMAR M; LAU D G; PAWLOWSKI S; WU W S
Patent Family (1 patents, 1 countries)

Patent			Application			
Number	Kind	Date	Number	Kind	Date	Update
US 6263397	B1	20010717	US 1996777308	A	19961227	200149 B
			US 1998206995	A	19981207	

Priority Applications (no., kind, date): US 1996777308 A 19961227; US 1998206995 A 19981207

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 6263397	B1	EN	9	4	Continuation of application US 1996777308
					Continuation of patent US 5848279

Alerting Abstract ...NOVELTY - An **multiprocessor** system (105) in/output (I/O) agent (150) generates an **interrupt message** and **sends** it via chipset system bus (110). The message includes destination ID. Data involved is written to a **buffer** queue (125). The interrupt is written to the chipset interfacing the I/O agent and processor identified by the destination ID. The contents of the **buffer** queue are moved to main **memory** (130) before message delivery....125 **Buffer** queue...

...130 Main **memory**
...

...135 Interface between chipset and main **memory**

Original Publication Data by Authority

Original Abstracts:
...interrupt message. The I/O agent writes the data associated with the interrupt into the **buffer** queue inside the chipset. The chipset automatically flushes the contents of the **buffer** queue to the main **memory** before the interrupt message is delivered. The interrupt delivery mechanism avoids complexity and delay in...

Claims:
...an interrupt request by a device;depositing data associated with the interrupt request to a **buffer** queue;transmitting the interrupt request **on** a system bus via a transaction, the transaction characterizing the interrupt request;transferring the deposited data to a **memory** without a handshaking operation; andreceiving the interrupt request **from** the system bus by a processor.

16/3,K/8 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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0008480888 - Drawing available
WPI ACC NO: 1998-010130/199802
XRPX Acc No: N1998-007892
Cache buffer storage **coherence operation in multi-processor installation - transfers** buffer **row** memory **from PURGING to INVALID state upon completion of return to main** memory **from intervening state of sub-block access**
Patent Assignee: SIEMENS NIXDORF INFORM AG (SIEI)
Inventor: HEINRICHS H
Patent Family (2 patents, 19 countries)
Patent Application

Number	Kind	Date	Number	Kind	Date	Update
DE 19621108	A1	19971127	DE 19621108	A	19960524	199802 B
WO 1997045791	A1	19971204	WO 1997DE972	A	19970514	199803 E

Priority Applications (no., kind, date): DE 19621108 A 19960524

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
DE 19621108	A1	DE	6	1	
WO 1997045791	A1	DE	16		

National Designated States,Original: JP US
Regional Designated States,Original: AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE

Cache buffer storage **coherence operation in multi-processor installation...**

...transfers buffer **row** memory **from PURGING to INVALID state upon completion of return to main** memory **from intervening state of sub-block access**

Original Titles:
... **BUFFER STORAGE** OPERATING METHOD

Alerting Abstract ...The bus system linking the processors' **buffer** row memories to one another and to main **memory** allows a **memory** access during the address phase to distinguish access to an entire row or to a sub-block. The state diagram shows an INVALID state when the **buffer** row is not available, a PURGING state, and intervening states when data of the same address in main **memory** are not available. If a sub block **memory** access is in such a state the system switches to PURGING and initiates return of the **buffer** row to the main **memory** .
...

...ADVANTAGE - Method is faster and more robust than software solutions but requires no input/output **buffer storage** control as such.

Title Terms/Index Terms/Additional Words: **CACHE** ; ...

... **BUFFER** ; ...

... **STORAGE** ; ...

... **MEMORY** ;

Original Publication Data by Authority

Original Abstracts:
...The invention concerns a method of operating **buffer storage** systems in multi-processor central processing units **with coupling** by means **of bus** systems. The data transfer of an input-output system acting on a **memory** array which is located exclusively in a **buffer memory** is first interrupted, produces the marking PURGED, **and then** brings about re-writing in the main **memory** , whereupon the marking changes to INVALID and the **interrupted data transfer** can be repeated.

16/3,K/9 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0008148876 - Drawing available
WPI ACC NO: 1997-250078/199723
XRPX Acc No: N1997-206507
Multiprocessor system - indicates interruption location based on which data transfer to particular processor is terminated and initialisation of next processor is carried out by software control
Patent Assignee: NEC KOFU LTD (NIDE)
Inventor: SHIMIZU H
Patent Family (1 patents, 1 countries)

Patent		Application				
Number	Kind	Date	Number	Kind	Date	Update
JP 9081402	A	19970328	JP 1995235082	A	19950913	199723 B

Priority Applications (no., kind, date): JP 1995235082 A 19950913

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
JP 9081402	A	JA	4	5	

Alerting Abstract ...The system includes a share **memory** (4) which is connected with **multiple processors** (10-12) through a network (2). The data transfer between the **memory** and the processor is performed by a data transfer processor (3). When an interruption is generated in a specific processor during **data transfer** , the **interruption** generated location is indicated to the data transfer process...

16/3,K/10 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0007878642 - Drawing available
WPI ACC NO: 1996-510178/199651
XRPX Acc No: N1996-430048
CPU performance monitoring system for multiprocessor - has special purpose register which holds acquired state information at predefined time irrespective of whether interruption demand to multiprocessor is accepted
Patent Assignee: IBM CORP (IBMC); INT BUSINESS MACHINES CORP (IBMC)
Inventor: ARNDT R L; EDWARD F W; FRANK E L; LEVINE F E; SILHA E J; WELBON E H
Patent Family (2 patents, 2 countries)

Patent		Application				
Number	Kind	Date	Number	Kind	Date	Update
JP 8263310	A	19961011	JP 1995316705	A	19951205	199651 B
US 5802378	A	19980901	US 1994358220	A	19941216	199842 E
			US 1996675427	A	19960626	

Priority Applications (no., kind, date): US 1996675427 A 19960626; US 1994358220 A 19941216

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
JP 8263310	A	JA	13	4	
US 5802378	A	EN			Continuation of application US 1994358220

Alerting Abstract ...register. An interruption processing mechanism transfers the registered state information from the register into a **memory** of the multiprocessor environment...

Original Publication Data by Authority

Original Abstracts:

...time base mechanism requests that the machine state be recorded, the performance monitor then immediately **stores** the machine state **values** in the special purpose registers. Thus, the state of the each CPU in the MP...

...request to the interrupt handler and, if interrupts are enabled, the machine state data is **stored** for post-processing, **or** the like. However, if the interrupt handler has disabled interrupts, then the machine state data...

...to the same point in time) is then read from the special purpose registers into **memory** , or the like, **for** post-processing.

Claims:

...receiving said notification signal, and for placing said state information in at least one register **regardless** of whether **interrupts** are masked or not;means, in each said CPU for issuing a transfer request signal to transfer said state information from said register to a memory in said **multiprocessor** system; andan interrupt handling mechanism, in each said CPU, which initiates a substantially immediate...

...register to said memory when interrupt masking is not present, and which defers transfer of **said** state **information** , irrespective of said **transfer request signal** , from said register **to** said memory when **interrupt** masking is present;wherein said state **information** corresponding to **said** predetermined point in time is maintained, independent of **whether** any of said **interrupt** handling mechanisms are responding to said transfer request signal.

16/3,K/11 (Item 9 from file: 350)

0007136571 - Drawing available
WPI ACC NO: 1995-169936/199522
Related WPI Acc No: 1994-048383; 1995-275212; 1996-425010; 1998-322149; 1994-319030
XRPX Acc No: N1995-133252

Multiprocessor programmable interrupt controller system adapted to functional redundancy checking - has interrupt bus separated and distinct from system bus and I-O interrupt delivery unit connected to interrupt bus and to set of IRQ pins

Patent Assignee: INTEL CORP (ITLC)
Inventor: CARSON D G; NIZAR P.K; PAPWORTH D; SARANGDHAR N V
Patent Family (1 patents, 1 countries)

Patent			Application			
Number	Kind	Date	Number	Kind	Date	Update
US 5410710	A	19950425	US 1990632149	A	19901221	199522 B
			US 19938074	A	19930122	
			US 1993176136	A	19931230	

Priority Applications (no., kind, date): US 19938074 A 19930122; US 1990632149 A 19901221; US 1993176136 A 19931230
Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 5410710	A	EN	44	43	C-I-P of application US 1990632149
					C-I-P of application US 19938074
					C-I-P of patent US 5283904

Original Publication Data by Authority

Original Abstracts:
...a functional redundant checking (FRC) unit, has a synchronous interrupt bus, distinct from the system (**memory**) bus, with an **interrupt** bus clock that has a frequency that is a subharmonic of the FRC unit master...
Claims:
...master processor and a checker processor operating with common core and CPU bus clocks, the **multiprocessor** programmable **interrupt** controller system comprising: a) an interrupt bus synchronizing clock signal with a rate that is less than one half the common core clock rate; b) a synchronous **interrupt** bus **for transmitting** the **interrupt** bus **synchronizing** clock signal, for **interrupt** request **data** communication, **and** for arbitration messages for **control** of the **interrupt** bus; c) an interrupt delivery unit (IDU) connected to the interrupt bus comprising: i) a...

16/3,K/12 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0006922076 - Drawing available
WPI ACC NO: 1994-319030/199440
Related WPI Acc No: 1994-048383; 1995-275212; 1995-169936; 1998-322149; 1996-425010
XRPX Acc No: N1994-250636
Programmable multi-processor interrupt controller system with processor integrated local interrupt controller - has Input-Output interrupt controller for receiving interrupt request from I-O subsystem, and multiple processor interrupt controllers each associated with specific processor for dispensing of accepted interrupts
Patent Assignee: INTEL CORP (ITLC)
Inventor: CARSON D; NIZAR P K
Patent Family (9 patents, 5 countries)

Patent			Application			
Number	Kind	Date	Number	Kind	Date	Update
GB 2277388	A	19941026	GB 19942811	A	19940214	199440 B

DE 4413459 A1 19941020 DE 4413459 A 19940418 199441 E
US 5613128 A 19970318 US 1990632149 A 19901221 199717 E
US 19938074 A 19930122
US 199349515 A 19930419
US 1996643734 A 19960506
GB 2277388 B 19970813 GB 19942811 A 19940214 199735 E
IT 1270035 B 19970428 IT 1994MI730 A 19940415 199745 E
US 5696976 A 19971209 US 1990632149 A 19901221 199804 E
US 19938074 A 19930122
US 199349515 A 19930419
US 1996643734 A 19960506
US 1996710452 A 19960917
US 5701496 A 19971223 US 1990632149 A 19901221 199806 E
US 19938074 A 19930122
US 199349515 A 19930419
US 1996643734 A 19960506
US 1996710451 A 19960917
SG 48803 A1 19980518 SG 19961861 A 19940214 199834 E
DE 4413459 C2 20000406 DE 4413459 A 19940418 200021 E

Priority Applications (no., kind, date): US 1996710452 A 19960917; US 1996710451 A 19960917; US 1996643734 A 19960506; US 19938074 A 19930122; US 1990632149 A 19901221; US 199349515 A 19930419

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
GB 2277388	A	EN	62	21	
DE 4413459	A1	DE	28	21	
US 5613128	A	EN	24	21	Continuation of application US 1990632149 C-I-P of application US 19938074 Continuation of application US 199349515 C-I-P of patent US 5283904
US 5696976	A	EN	23	21	Continuation of application US 1990632149 C-I-P of application US 19938074 Continuation of application US 199349515 Continuation of application US 1996643734 C-I-P of patent US 5283904 Continuation of patent US 5613128
US 5701496	A	EN	23	21	Continuation of application US 1990632149 C-I-P of application US 19938074 Continuation of application US 199349515 Continuation of application US 1996643734 C-I-P of patent US 5283904 Continuation of patent US 5613128
SG 48803	A1	EN			

Original Publication Data by Authority

Claims:
... **The** multi-processor programmable interrupt controller system includes an I/O interrupt controller for receiving interrupt request from an I/ **O subsystem** , multiple processor interrupt controllers, each associated with a specific processor for dispensing of accepted interrupts. An interrupt controller bus is provided primarily **for** the **transmission** of interrupt request between interrupt controller units and for bus and priority arbitration, using a...

... The system is implemented, in part by incorporating **the** processor interrupt controller **with** its **associated** processor into a single integrated circuit. The common system bus which normally carries all **system** traffic is not **used** for **interrupt** request **messages** . The interrupt controller bus is used for this purpose and thus results in a more...

...coupled to the interrupt bus and to a first processor, the first controller having a **register** that stores a value which controls acceptance of an interrupt request; a second controller coupled...

...controller including logic that broadcasts a remote read message on the interrupt bus that requests **the** value stored in the register from the first controller; the first controller further including logic...

...to the remote read message, the second controller receiving the value across the interrupt bus.

A ...

...A multi-processor programmable interrupt controller system, comprising; ul> (a) a common system bus; (b) an interrupt bus; (c) at least **one** I/ **O** interrupt controller, **coupled** to said interrupt bus, operable to receive an interrupt request signal and, **responsive** thereto, **to** transmit formatted interrupt requests on said interrupt bus; (d) a multiplicity of processors, coupled to...
...ports; and (e) a multiplicity of local processor interrupt controllers, each coupled to said data, **address** , **and** control ports of an associated one of said processors and each coupled to said interrupt...

...interrupt bus and to accept those which said associated processor is eligible to service, to **broadcast** on **said** interrupt **bus** an acceptance signal upon said acceptance, to queue said accepted interrupt requests, and to deliver...

...to the interrupt bus and to a first processor, the first interrupt controller having a **control** register that stores a value which controls acceptance of an interrupt request; a second interrupt...

...interrupt controller including logic that broadcasts a remote read message on the interrupt bus that **requests** the value stored in the control register from the first interrupt controller; and the first i

16/3,K/13 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0006368652 - Drawing available
WPI ACC NO: 1993-167248/199320
XRPX Acc No: N1993-128068

Multi-processor system with dual port memory **malfunction detector - confirms status of interrupt request signal generating function of one processor.**

Patent Assignee: MINOLTA CAMERA KK (MIOC)
Inventor: TOMITA H

Patent Family (1 patents, 1 countries)

Patent			Application			
Number	Kind	Date	Number	Kind	Date	Update
US 5210863	A	19930511	US 1990473818	A	19900202	199320 B

Priority Applications (no., kind, date): JP 198924957 A 19890203

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 5210863	A	EN	9	4	

Multi-processor system with dual port memory **malfunction detector...**

Original Titles:
Multi-processor system for detecting a malfunction of a dual port **memory**

Alerting Abstract ...They multi-processor system has two processors connected through a dual port **memory** which receives from one of the processors an interruption request signal together with the data to be transmitted to the other processor. The dual port **memory** then generates an interrupt signal for the other processor so that the other processor can fetch the data from the dual port **memory** using an interrupt procedure...

...The one processor also receives the interrupt signal transmitted by the dual port **memory** in order to confirm the status of the interrupt signal generating function of the dual port **memory** .$
...

...ADVANTAGE - Detects failures in interrupt signal generating function of **memory** .

Title Terms.../Index Terms/Additional Words: **MEMORY** ;

Original Publication Data by Authority

Original Abstracts:
A multi-processor system wherein two processors are connected through a dual port **memory** which receives from **one** of the processors an interruption request signal together with the data to be transmitted to the other processor. The dual port **memory** then generates an **interrupt** signal for the other processor so that the other processor can fetch the data from the dual port **memory** using an interrupt **procedure** . The one processor also receives the interrupt signal transmitted by the dual port **memory** in order to **confirm** the status of the interrupt signal generating function of the dual port **memory**.

Claims:

A **multi - processor system , comprising** : two processors; a dual port **memory** means **for** receiving from one of the processors an interrupt request **signal** together with **data** to be transmitted to the other processor and for **transmitting** an **interrupt** signal **to** said other processor; said other processor having means for fetching said data from said dual port **memory** means **during** an interrupt procedure responsive to said interrupt signal; and means, in said one processor and responsive to said interrupt signal transmitted from the dual port **memory** means **to** said other processor in response to said interrupt request signal generated from said one processor, for confirming the status of the interrupt signal generating function of said dual port **memory** means.

16/3,K/14 (Item 12 from file: 350)

DIALOG(R)File 350:Derwent WPIX

0006285027 - Drawing available

WPI ACC NO: 1993-078517/199310

XRPX Acc No: N1993-060242

Data processing with bidirectional data bus reservation priority control - using token to allow holding requesting device priority over other requesting devices

Patent Assignee: IBM CORP (IBMC); INT BUSINESS MACHINES CORP (IBMC)

Inventor: HERZL R D; SCHROTER D A

Patent Family (4 patents, 5 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
EP 531003	A1	19930310	EP 1992307484	A	19920814	199310 B
JP 5242022	A	19930921	JP 1992228140	A	19920827	199342 E
US 5835714	A	19981110	US 1991755237	A	19910905	199901 E
			US 1995459875	A	19950602	
US 5953510	A	19990914	US 1991755237	A	19910905	199944 E

Priority Applications (no., kind, date): US 1995459875 A 19950602; US 1991755237 A 19910905

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
EP 531003	A1	EN	10	4	
Regional Designated States,Original: DE FR GB					
US 5835714	A	EN			Continuation of application US 1991755237

Original Titles:

...Method and apparatus for reservation of data buses between multiple **storage** control elements...

Alerting Abstract ...The method involves controlling data transfer between **storage** control elements (SCEs) in a multiprocessor system. Each SCE is assigned a default bidirectional (BIDI...

Original Publication Data by Authority

Original Abstracts:
A data bus reservation system controls data transfer between **storage** control elements (SCEs) **in** a multi-processor system. Each SCE is assigned a default bidirectional (BIDI) data bus for...

...A data bus reservation system controls data transfer between **storage** control elements (SCEs) in a multi-processor system. **Each** SCE is assigned a default bidirectional (BIDI) data bus for transfer of data. If a...

...A data bus reservation system controls data transfer between **storage** control elements (SCEs) in a multi-processor system. Each SCE is assigned a **default** bidirectional (BIDI) data bus for transfer of data. If a request for data transfer is...

Claims:
...multi-processor data processing system containing a plurality of data buses interconnecting a plurality of **storage** control **elements** , said method comprising:</br> assigning each of said **storage** control elements a **default** data bus;</br> passing a token from one **storage** control element to another upon **the** occurrence of a machine cycle;</br> detecting a request for data transfer from one of said **storage** control elements, said **storage** control element being **a** requesting source;</br> reserving **said** requesting source's default data bus for said requested data transfer when all of said...

...multi-processor data processing system containing a plurality of data buses interconnecting a plurality of **storage** control elements, said method comprising the steps of:assigning each of said **storage** control elements **a** default data bus;passing a token from one **storage** control element to another upon **an** occurrence of a machine cycle;detecting a request for data transfer from one **of** said **storage** control elements, said one of said **storage** control elements being a requesting source;reserving said requesting source's default data bus **for** said requested data transfer when all **of** said plurality of data buses are available;delaying said data transfer if all of said...
...then attempting to reserve an alternate data bus,wherein data to be transferred from one **storage** control element to a second **storage** control element of said plurality of **storage** control elements spends at least one machine cycle in a data bus being used for the **data** transfer,wherein said plurality of **storage** control elements include first and second **storage** control elements and said plurality of data buses includes first and second data buses, said method further comprising the steps of:designating said first **storage** control element as a master and **said** second **storage** control element as a slave, said first data bus being assigned as the default data bus for said first **storage** control element and said **second** data bus being assigned as the default data **bus** for said second **storage** control element,wherein said first **storage** control element includes first token control logic and said **second** **storage** control element includes second token control logic, said method further comprising the step of activating said **first** token control logic and deactivating said second **token** control logic after said first **storage** control element is designated **said** master and said second **storage** control element is designated said slave.

...

...multi-processor data processing system containing a plurality of data buses interconnecting a plurality of **storage** control elements, said method comprising the steps of:assigning each of said **storage** control elements a default data bus;passing a token from one **storage** control **element** **to** another upon an occurrence of a machine cycle;detecting a request for data **transfer** from one of said **storage** control elements, said one of said **storage** control elements **being** a requesting source;reserving said requesting source's default data bus for said **requested** data transfer when all of said plurality of **data** buses are available; **delaying** said **data** **transfer** if all of said plurality of data **buses** are not available until said token **is** passed to said requesting source and at least one of said data buses is available...

...then attempting to reserve an alternate data bus,wherein data to be transferred from one **storage** control element to a second **storage** control element of said plurality of **storage** control elements spends at least one machine cycle in a data bus being used for

16/3,K/15 (Item 13 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0005992164 - Drawing available
WPI ACC NO: 1992-226326/199227
XRPX Acc No: N1992-172050
Inter processor communications for multiprocessor system - includes second CPU designating memory **locations assigned to first CPU and writing their addresses into registers**
Patent Assignee: APPLE COMPUTER INC (APPY)
Inventor: MACDOUGALL M H
Patent Family (1 patents, 1 countries)

Patent			Application			
Number	Kind	Date	Number	Kind	Date	Update
US 5123094	A	19920616	US 1990471093	A	19900126	199227 B

Priority Applications (no., kind, date): US 1990471093 A 19900126

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 5123094	A	EN	9	7	

...includes second CPU designating memory **locations assigned to first CPU and writing their addresses into registers**

Original Titles:
Interprocessor communications includes second CPU designating **memory** locations assigned to first CPU and writing their addresses into registers

Alerting Abstract ...The method for performing inter-processor communications in a **multiprocessor** system combines the sending of a message with the **sending** of a **message** **interrupt**. **Messages** are exchanged through a shared **memory** organised into pages, each of which may be 'owned' by a processor. When a sending processor executes a **store** instruction that **stores** its operand to a **memory** area owned by a destination processor, a **message** **interrupt** is presented to the

destination processor...

...If the destination processor is interrupt enabled, the operand of the **store** instruction is **stored** at the address specified by the **store** instruction and that address is **stored** in a register of the destination processor. Execution of the **store** instruction by the sending processor then completes...

Title Terms.../Index Terms/Additional Words: **MEMORY** ;

Original Publication Data by Authority

Original Abstracts:

A method for performing inter-processor communications in a **multiprocessor** system combines the sending of a message with the **sending** of a **message interrupt** . **Messages** are exchanged through a shared **memory** organized into pages, each of which may be "owned" by a processor. When a sending processor executes a **store** instruction that **stores** its operand to a **memory** area owned by a destination processor, a **message interrupt** is presented to the destination processor. If the destination processor is interrupt enabled, the operand of the **store** instruction is **stored** at the address specified by the **store** instruction and that address is **stored** in a register of the destination processor. Execution of the **store** instruction by the sending processor then completes.

Patent Fulltext

File 348:EUROPEAN PATENTS 1978-2007/ 200729
(c) 2007 European Patent Office
File 349:PCT FULLTEXT 1979-2007/UB=20070726UT=20070719
(c) 2007 WIPO/Thomson

Set	Items	Description
S1	14858	MULTIPROCESSOR??? OR MULTI???()PROCESSOR???
S2	1617694	IMPORT?? OR IMPORTING OR EXPORT??? OR SEND??? OR TRANSFER? ? OR TRANSFERR??? OR COPY??? OR TRANSMIT? OR TRANSMISSION? ? - OR DISPATCH???
S3	50620	S2(3N)(SUSPEND? OR STALL??? OR DISCONTINU??? OR DELAY??? OR POSTPON??? OR DEFER??? OR INTERRUPT??? OR ABANDON?? OR HALT?-?? OR TERMINAT??? OR CEASE? ? OR CEASING OR DISRUPT???)
S4	2713237	DATA OR INFO OR INFORMATION OR MESSAGE? OR REPORT?
S5	53366	S4(3N)(SUSPEND? OR STALL??? OR DISCONTINU??? OR DELAY??? OR POSTPON??? OR DEFER??? OR INTERRUPT??? OR ABANDON?? OR HALT?-?? OR TERMINAT??? OR CEASE? ? OR CEASING OR DISRUPT???)
S6	1033860	BUFFER? OR CACHE? OR MEMORY OR STOR?
S7	3729	S5(5N)(PRIOR OR BEFORE???? OR PREVIOUS? OR PROCED??? OR IN-ITIAL? OR EARLY OR EARLIER)
S8	4376	S3(5N)(AFTER???? OR LATER OR FOLLOW??? OR NEXT)
S9	19	S7(25N)S6(25N)S8
S10	1	S9(100N)S1
S11	12	S9 NOT AY=2002:2007
S12	11	S11 NOT S10

10/3,K/1 (Item 1 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00306062
Digital data processing system.
Digitales Datenverarbeitungssystem.
Systeme du traitement de donnees numeriques.
PATENT ASSIGNEE:
DATA GENERAL CORPORATION, (410940), Route 9, Westboro Massachusetts 01581 , (US), (applicant designated states: AT;BE;CH;DE;FR;GB;IT;LI;LU;NL;SE)
INVENTOR:
Bratt, Richard Glenn, 9 Brook Trail Road, Wayland Massachusetts 01778, (US)
Clancy, Gerald F., 13069 Jaccaranda Center, Saratoga California 95070, (US)
Gavrin, Edward S., Beaver Pond Road RFD 4, Lincoln Massachusetts 01773, (US)
Gruner, Ronald Hans, 112 Dublin Wood Drive, Cary North Carolina 27514, (US)
Mundie, Craig James, 136 Castlewood Drive, Cary North Carolina, (US)
Schleimer, Stephen I., 1208 Ellen Place, Chapel Hill North Carolina 27514 , (US)
Wallach, Steven J., 12436 Green Meadow Lane, Saratoga California 95070, (US)
LEGAL REPRESENTATIVE:
Robson, Aidan John et al (69471), Reddie & Grose 16 Theobalds Road, London WC1X 8PL, (GB)
PATENT (CC, No, Kind, Date): EP 300516 A2 890125 (Basic)
EP 300516 A3 890426
EP 300516 B1 931124
APPLICATION (CC, No, Date): EP 88200921 820521;
PRIORITY (CC, No, Date): US 266413 810522; US 266539 810522; US 266521 810522; US 266415 810522; US 266409 810522; US 266424 810522; US 266421 810522; US 266404 810522; US 266414 810522; US 266532 810522; US 266403 810522; US 266408 810522; US 266401 810522; US 266524 810522
DESIGNATED STATES: AT; BE; CH; DE; FR; GB; IT; LI; LU; NL; SE
RELATED PARENT NUMBER(S) - PN (AN):
EP 67556 (EP 823025960)
INTERNATIONAL PATENT CLASS (V7): G06F-009/46; G06F-012/14;
ABSTRACT WORD COUNT: 122

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text Language Update Word Count
CLAIMS B (English) EPBBF1 1018
CLAIMS B (German) EPBBF1 868
CLAIMS B (French) EPBBF1 1115
SPEC B (English) EPBBF1 154256
Total word count - document A 0
Total word count - document B 157257
Total word count - documents A + B 157257

...SPECIFICATION for the purposes of CS 10110's protection mechanisms. Each

domain is defined by a **set** of procedures having access to objects within that domain for their execution. Each object has a single domain of execution in which it **is** executed if it is a **procedure** object, or used, if it is a **data** object. CS 10110 is said **to** be operating in a particular domain if it is executing a procedure having that domain...

12/3,K/1 (Item 1 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01011067
A DSP-based, multi-bus, multiplexing communications adapter
Signalprozessorgestutzter Mehrfachbus-Kommunikationsadapter mit Multiplex
Adapteur de communications a multiplexage a bus multiple, base sur un DSP
PATENT ASSIGNEE:
International Business Machines Corporation, (200120), New Orchard Road, Armonk, N.Y. 10504, (US), (Proprietor designated states: all)
INVENTOR:
Andrews, Lawrence P., 275 NE 24th Court, Boca Raton,Florida 33431, (US)
Beckman, Richard Clyde, 4901 NW 3rd Avenue, Boca Raton,Florida 33431, (US)
Eng, Robert Chih-Tsin, 18084 105th Avenue S., Boca Raton,Florida 33498, (US)
Linger, Judith Marie, 2895 SW 22nd Avenue No. 107, Delray Beach,Florida 33445, (US)
Petty, Joseph C., Jr., 9604 Richmond Circle, Boca Raton,Florida 33431, (US)
Sinibaldi, John Claude, 2850 NE 19th Street, Pompano Beach,Florida 33062, (US)
Turbeville, Gary L., 4999 NW 4th Avenue, Boca Raton,Florida 33431, (US)
Williams, Kevin Bradley, 861 Orchid Drive, Plantation,Florida 33317, (US)
LEGAL REPRESENTATIVE:
Ling, Christopher John (80401), IBM United Kingdom Limited, Intellectual Property Department, Hursley Park, Winchester,Hampshire SO21 2JN, (GB)
PATENT (CC, No, Kind, Date): EP 908830 A1 990414 (Basic)
EP 908830 B1 061102
APPLICATION (CC, No, Date): EP 98307454 980915;
PRIORITY (CC, No, Date): US 944209 971006
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS (V7): G06F-013/24;
INTERNATIONAL CLASSIFICATION (V8 + ATTRIBUTES):
IPC + Level Value Position Status Version Action Source Office:
G06F-0013/24 A I F B 20060101 19990205 H EP
ABSTRACT WORD COUNT: 124
NOTE:
Figure number on first page: 1

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text Language Update Word Count
CLAIMS A (English) 199915 901
CLAIMS B (English) 200644 771
CLAIMS B (German) 200644 711
CLAIMS B (French) 200644 936
SPEC A (English) 199915 6013
SPEC B (English) 200644 6134

Total word count - document A 6915
Total word count - document B 8552
Total word count - documents A + B 15467

...CLAIMS upon receipt of an acknowledgement from said host processor (53a) of a control block of **interrupt information previously** transmitted from said digital signal processor subsystem (12) to said second data **memory** (89).

5. A method as claimed in claim 4, wherein said control block is additionally transmitted upon accumulation of a predetermined maximum number of **interrupt** blocks **after transmission** to said second data **memory** (89) from said digital signal processor subsystem (12)of a **previously** transmitted control block of **interrupt information**.
6. A method as claimed in claim 4, wherein said control block is additionally transmitted when elapsed time following transmission to said second data **memory** (89) from said digital signal processor subsystem (12) of a **previously** transmitted control block of **interrupt information** reaches a predetermined value.
7. A method as claimed in claim 4, wherein said control block is additionally transmitted when elapsed time, **following** a first **interrupt** request occurring **after transmission** to said second data memory (89) from said digital signal processor subsystem (12) of a **previously** transmitted control block of **interrupt information**, reaches a predetermined level.
8. A method as claimed in claim 3, wherein said control block is transmitted upon accumulation of a predetermined maximum number of **interrupt** blocks **after transmission** to said second data **memory** (89) from said digital signal processor subsystem (12) of a **previously** transmitted control block of **interrupt information**.
9. A method as claimed in claim 3, wherein said control block is transmitted when elapsed time following transmission to said second data **memory** (89) from said digital signal processor subsystem (12) of a **previously** transmitted control block of **interrupt information** reaches a predetermined value.
10. A method as claimed in claim 3, wherein said control block is transmitted when elapsed time, **following** a first **interrupt** request occurring **after transmission** to said second data **memory** (89) from said digital signal processor subsystem (12) of a **previously** transmitted control block of **interrupt information**, reaches a predetermined level.
11. Apparatus comprising:

network interface means (24) for connection to a...

...CLAIMS wherein said data signal processor subsystem (12) sends said interrupt information to said second data **memory** (89) by means of direct **memory** access.

3. A method as claimed in claim 1, wherein said control block is transmitted upon receipt of an acknowledgement from said host processor (53a) of a control block of **interrupt information previously** transmitted from said digital signal processor subsystem (12) to said second data 1memory (89).
4. A method as claimed in claim 3, wherein said control block is additionally transmitted upon accumulation of a predetermined maximum number of **interrupt** blocks **after transmission** to said second data **memory** (89) from said digital signal processor subsystem (12)

of a **previously** transmitted control block of **interrupt information**.

5. A method as claimed in claim 3, wherein said control block is additionally transmitted when elapsed time following transmission to said second data **memory** (89) from said digital signal processor subsystem (12) of a **previously** transmitted control block of **interrupt information** reaches a predetermined value.
6. A method as claimed in claim 3, wherein said control block is additionally transmitted when elapsed time, **following** a first **interrupt** request occurring **after transmission** to said second data memory (89) from said digital signal processor subsystem (12) of a **previously** transmitted control block of **interrupt information**, reaches a predetermined level.
7. A method as claimed in claim 1, wherein said control block is transmitted upon accumulation of a predetermined maximum number of **interrupt** blocks **after transmission** to said second data **memory** (89) from said digital signal processor subsystem (12) of a **previously** transmitted control block of **interrupt information**.
8. A method as claimed in claim 1, wherein said control block is transmitted when elapsed time following transmission to said second data **memory** (89) from said digital signal processor subsystem (12) of a **previously** transmitted control block of **interrupt information** reaches a predetermined value.
9. A method as claimed in claim 1, wherein said control block is transmitted when elapsed time, **following** a first **interrupt** request occurring **after transmission** to said second data **memory** (89) from said digital signal processor subsystem (12) of a **previously** transmitted control block of **interrupt information**, reaches a predetermined level.
10. Apparatus comprising:first and second communications adapters (10), with each...

12/3,K/2 (Item 2 from file: 348)

00750446

Automatic call distribution system with user definable logging and method therefor

Automatisches Anrufverteilsystem mit anwenderdefinierbarer Protokollierung und Verfahren hierfur

Systeme automatique pour distribuer des appels telephoniques avec protocole determinable par utilisateur et procede pour sa mise en oeuvre

PATENT ASSIGNEE:
ROCKWELL INTERNATIONAL CORPORATION, (1727901), 1431 Opus Place, Downers Grove, Illinois 60515, (US), (Proprietor designated states: all)
INVENTOR:
Sunderman, Kurt E., 906 Longmeadow Drive, Elburn, Illinois 60119, (US)
Michelson, Mark J., 2N078 Mulhern Drive, Elburn, Illinois 60119, (US)
Lenihan, John P., 1605 Whitman Lane, Wheaton, Illinois 60187, (US)
LEGAL REPRESENTATIVE:
Degwert, Hartmut, Dipl.-Phys. et al (38536), Prinz & Partner GbR, Manzingerweg 7, 81241 Munchen, (DE)

PATENT (CC, No, Kind, Date): EP 707405 A2 960417 (Basic)

EP 707405 A3 960424
EP 707405 B1 040526
APPLICATION (CC, No, Date): EP 95114980 950922;
PRIORITY (CC, No, Date): US 311636 940923
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS (V7): H04M-003/523; H04M-003/42
ABSTRACT WORD COUNT: 195
NOTE:
Figure number on first page: 1

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text Language Update Word Count
CLAIMS A (English) EPAB96 756
CLAIMS B (English) 200422 341
CLAIMS B (German) 200422 292
CLAIMS B (French) 200422 359
SPEC A (English) EPAB96 2577
SPEC B (English) 200422 2543
Total word count - document A 3334
Total word count - document B 3535
Total word count - documents A + B 6869

...SPECIFICATION abandons the call, the CPU 116 generates data indicating that the call has been abandoned. **After** a predetermined time, this " **abandoned** " data is then **transmitted** to and **stored** in the data computer 108.
Unfortunately, the operator 306 of the system 100 may want...

...heard the announcement 25. With the above vector, however, the operator 306 cannot obtain this **information** . Callers who **abandoned** the call **before** hearing the announcement 25, callers who heard only the announcement 25 and callers who heard...

...SPECIFICATION abandons the call, the CPU 116 generates data indicating that the call has been abandoned. **After** a predetermined time, this " **abandoned** " data is then **transmitted** to and **stored** in the data computer 108.
Unfortunately, the operator 306 of the system 100 may want...

...heard the announcement 25. With the above vector, however, the operator 306 cannot obtain this **information** . Callers who **abandoned** the call **before** hearing the announcement 25, callers who heard only the announcement 25 and callers who heard...

12/3,K/3 (Item 3 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00481342
A control system for multi-processor system
Steuerungsanlage fur ein Mehrprozessorsystem
Systeme de controle pour un systeme multiprocesseur
PATENT ASSIGNEE:
FUJITSU LIMITED, (211460), 1015, Kamikodanaka, Nakahara-ku, Kawasaki-shi,

Kanagawa 211, (JP), (applicant designated states: DE;ES;FR;GB)
INVENTOR:
Kimura, Makoto, 8-14, Kobayashi-Kita 5-chome, Inzaimachi, Inba-Gun, Chiba, 270-13, (JP)
LEGAL REPRESENTATIVE:
Billington, Lawrence Emlyn et al (28331), HASELTINE LAKE & CO Hazlitt House 28 Southampton Buildings Chancery Lane, London WC2A 1AT, (GB)
PATENT (CC, No, Kind, Date): EP 446077 A2 910911 (Basic)
EP 446077 A3 930107
EP 446077 B1 960918
APPLICATION (CC, No, Date): EP 91301976 910311;
PRIORITY (CC, No, Date): JP 9059070 900309
DESIGNATED STATES: DE; ES; FR; GB
INTERNATIONAL PATENT CLASS (V7): G06F-015/16; G06F-013/38; G06F-013/10; G06F-015/17;
ABSTRACT WORD COUNT: 110

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text Language Update Word Count
CLAIMS A (English) EPABF1 1742
CLAIMS B (English) EPAB96 1808
CLAIMS B (German) EPAB96 1618
CLAIMS B (French) EPAB96 2198
SPEC A (English) EPABF1 6359
SPEC B (English) EPAB96 6481
Total word count - document A 8101
Total word count - document B 12105
Total word count - documents A + B 20206

...SPECIFICATION interrupt is acceptable.
A mechanism of an interruption occurrence for a single PM is as **follows** .
When a DVCm **transmits** an **interruption** request to a PM, APU 21 (comprising a firmware operating on the APU) **previously stores** the detailed **interruption information** in the area of MSU 12 designated by PM upon an issuance of an I...

...SPECIFICATION interrupt is acceptable.
A mechanism of an interruption occurrence for a single PM is as **follows** .
When a DVCm **transmits** an **interruption** request to a PM, APU 21 (comprising a firmware operating on the APU) **previously stores** the detailed **interruption information** in the area of MSU 12 designated by PM upon an issuance of an I...

12/3,K/4 (Item 4 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00480869
Integrated data link controller with synchronous link interface and asynchronous host processor interface
Integrierte Datenubertragungsstreckensteuerung mit synchroner Leitungsschnittstelle und asynchroner Host-Prozessor-Schnittstelle

Dispositif integre de commande d'une voie de donnees avec interface synchrone de liaison et interface asynchrone avec le processeur hote

PATENT ASSIGNEE:
International Business Machines Corporation, (200120), Old Orchard Road, Armonk, N.Y. 10504, (US), (applicant designated states: BE;CH;DE;ES;FR;GB;IT;LI;NL;SE)

INVENTOR:
Farrell, Joseph Kevin, 4713 Tortoise Shell Drive, Boca Raton, Florida 33487, (US)
Gordon, Jeffrey Scott, 5107 Woodmere Drive, No. 203 Centreville, Virginia 22020, (US)
Jenness, Robert V., 1499 West Royal Palm Road, Boca Raton, Florida 33486, (US)
Kuhl, Daniel C., 16416 Cherry Way, Delray Beach, Florida 33484, (US)
Lee, Timothy Vincent, 1798 S.W. 11th Street, Boca Raton, Florida 33486, (US)
Parker, Tony Edwin, 1745 N.W. 4th Avenue. Unit No. 5, Boca Raton, Florida 33432-1545, (US)

LEGAL REPRESENTATIVE:
Burt, Roger James, Dr. (52152), IBM United Kingdom Limited Intellectual Property Department Hursley Park, Winchester Hampshire SO21 2JN, (GB)

PATENT (CC, No, Kind, Date): EP 447054 A2 910918 (Basic)
EP 447054 A3 951025
EP 447054 B1 990107

APPLICATION (CC, No, Date): EP 91301499 910225;
PRIORITY (CC, No, Date): US 495810 900315
DESIGNATED STATES: BE; CH; DE; ES; FR; GB; IT; LI; NL; SE
INTERNATIONAL PATENT CLASS (V7): H04L-029/06;
ABSTRACT WORD COUNT: 233

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	9901	4873
CLAIMS B	(German)	9901	4464
CLAIMS B	(French)	9901	6004
SPEC B	(English)	9901	66251

Total word count - document A 0
Total word count - document B 81592
Total word count - documents A + B 81592

12/3,K/5 (Item 5 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00397342
Method and means for error checking of dram-control signals between system modules.
Fehlerprufungsverfahren und -mittel fur dynamische RAM-Kontrollsignale zwischen Systemmodulen.
Methode et moyens de verification d'erreur pour les signaux de controle de RAM dynamiques entre des modules d'un systeme.

PATENT ASSIGNEE:
DIGITAL EQUIPMENT CORPORATION, (313081), 111 Powdermill Road, Maynard Massachusetts 01754-1418, (US), (applicant designated states:

AT;BE;CH;DE;DK;ES;FR;GB;GR;IT;LI;LU;NL;SE)
INVENTOR:
Gagliardo, Michael A., 32 Pal Drive, Shrewsbury, Massachusetts 01545, (US)
Tessari, James E., 222 Mistic Valley Parkway, Arlington, Massachusetts 01752, (US)
Collins, Hansel A., 901C Ridgefield Circle, Clinton, Massachusetts 01510, (US)
Lynch, John, 46 Bent Avenue, Wayland, Massachusetts 01778, (US)
Chinnaswamy, Kumar, 12C Country Club Lane, Milford, Massachusetts 01757, (US)
LEGAL REPRESENTATIVE:
Hale, Peter et al (60281), Kilburn & Strode 30 John Street, London WC1N 2DD, (GB)
PATENT (CC, No, Kind, Date): EP 382390 A2 900816 (Basic)
EP 382390 A3 911127
APPLICATION (CC, No, Date): EP 90300955 900130;
PRIORITY (CC, No, Date): US 306836 890203
DESIGNATED STATES: AT; BE; CH; DE; DK; ES; FR; GB; GR; IT; LI; LU; NL; SE
INTERNATIONAL PATENT CLASS (V7): G06F-011/10; G06F-013/42;
ABSTRACT WORD COUNT: 272

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text Language Update Word Count
CLAIMS A (English) EPABF1 810
SPEC A (English) EPABF1 11925
Total word count - document A 12735
Total word count - document B 0
Total word count - documents A + B 12735

...CLAIMS the means for comparing include means (295) for enabling the comparing of the parity of **previously transmitted data after** a **delay** of a predetermined period subsequent to a transition in the control signal.
11. A system...

...13, wherein the data includes control signals for controlling access to a dynamic random access **memory** (DRAM).
15. A system as claimed in claim 14, wherein the control signals include a...

...or 16, wherein the means for comparing include means (259) for enabling the comparison of **previously transmitted data after** a **delay** of a predetermined period subsequent to a transition in a selected one of the control...

12/3,K/6 (Item 6 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00306058
Digital data processing system.
Digitales Datenverarbeitungssystem.
Systeme de traitement de donnees numeriques.

PATENT ASSIGNEE:
DATA GENERAL CORPORATION, (410940), Route 9, Westboro Massachusetts 01581 , (US), (applicant designated states: AT;BE;CH;DE;FR;GB;IT;LI;LU;NL;SE)
INVENTOR:
Bachman, Brett L., 214 W. Canton Street Suite 4, Boston Massachusetts 02116, (US)
Bernstein, David H., 41 Bay Colony Drive, Ashland Massachusetts 01721, (US)
Bratt, Richard Glenn, 9 Brook Trail Road, Wayland Massachusetts 01778, (US)
Clancy, Gerald F., 13069 Jaccaranda Center, Saratoga California 95070, (US)
Gavrin, Edward S., Beaver Pond Road RFD 4, Lincoln Massachusetts 01773, (US)
Gruner, Ronald Hans, 112 Dublin Wood Drive, Cary North Carolina 27514, (US)
Jones, Thomas M. Jones, 300 Reade Road, Chapel Hill North Carolina 27514, (US)
Katz, Lawrence H., 10943 S. Forest Ridge Road, Oregon City Oregon 97045, (US)
Mundie, Craig James, 136 Castlewood Drive, Cary North Carolina, (US)
Pilat, John F., 1308 Ravenhurst Drive, Raleigh North Carolina 27609, (US)
Richmond, Michael S., Fearringtn Post Box 51, Pittsboro North Carolina 27312, (US)
Schleimer Stephen I., 1208 Ellen Place, Chapel Hill North Carolina 27514, (US)
Wallach, Steven J., 12436 Green Meadow Lane, Saratoga California 95070, (US)
Wallach, Walter, A., Jr., 1336 Medfield Road, Raleigh North Carolina 27607, (US)
LEGAL REPRESENTATIVE:
Robson, Aidan John et al (69471), Reddie & Grose 16 Theobalds Road, London WC1X 8PL, (GB)
PATENT (CC, No, Kind, Date): EP 290111 A2 881109 (Basic)
EP 290111 A3 890503
EP 290111 B1 931222
APPLICATION (CC, No, Date): EP 88200917 820521;
PRIORITY (CC, No, Date): US 266404 810522
DESIGNATED STATES: AT; BE; CH; DE; FR; GB; IT; LI; LU; NL; SE
RELATED PARENT NUMBER(S) - PN (AN):
EP 67556 (EP 823025960)
INTERNATIONAL PATENT CLASS (V7): G06F-009/30;
ABSTRACT WORD COUNT: 123

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text Language Update Word Count
CLAIMS B (English) EPBBF1 1044
CLAIMS B (German) EPBBF1 890
CLAIMS B (French) EPBBF1 1185
SPEC B (English) EPBBF1 154314
Total word count - document A 0
Total word count - document B 157433
Total word count - documents A + B 157433

...SPECIFICATION interrupt, state of first interrupt is transferred from SS

504 to EUS 512 and completed. After completion of first interrupt, state of the original SOP is transferred from SOP Stack 514 to EUS 512 and...is a uniquely identifiable portion of "data space" accessible to CS 10110. An object may be regarded as a container for information and may contain data or procedure information or both. An object may contain for example, an entire program, or set of procedures, or a single bit of...

...to CS 10110, and the information contained in an object need not be contiguously located in that object.

A domain is a state of operation of CS 10110 for the purposes...

...execute a second program. IOS 10116 would fetch the requested information from ED 10124 and transfer it into MEM 10112. At some time after IOS 10116 notifies JP 10114 that the requested information is available in MEM 10112, JP 10114 could suspend execution of the second program and resume execution of the first program.

e. Multi-Language Operation

As...10110's addressing structure includes a mechanism for recognizing Names as they appear in an instruction stream and Name Tables containing directions for resolving Names to AON logical addresses. AON logical...to operations.

KOSMAS 10334 Stack Header 10410 thereby contains information for locating certain important points in KOSMAS 10334's structure, and for locating certain information pertinent to executing procedures in KOS domain.

Each Frame Header 10414 contains at least the following information :

(1) offsets, relative to the Frame Header 10414, indicating the locations of Frame Headers 10414 of the previous and next frames of KOSMAS 10334;

(2...for loading the data from MSB 20110 and its associated address into MC 20116's cache. This data is transferred into MC 20116's cache data store while the block address...

...20116's cache. If the transfer of data into MC 20116's cache replaces data previously resident in that cache, and that previous data is "dirty", that is has been written into so as to be different from an be written back into MSB 20110. This operation is performed through a Write Back File contained in MC 20116 and described below. In the event of such an operation, LM 20730 initiates a write back...

...as described below.

As will be described further in a following description, all MC 20116 cache load operations are full 4 word blocks. A request resulting in a MC 20116 cache...

...from MSB 20110 and corrects single bit errors. In the second, BC 20114 reads data stored in MA's 20112 during refresh operations and performs single bit error detection. Whenever an error is detected, during either read operations or refresh operations, BC 20114 makes a record of...

...error log is transferred to JP 10114 or IOS 10116 in the same manner as data stored in MSB 20110.

Referring finally to MA's 20112, each MA 20112 contains an array...

12/3,K/7 (Item 7 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00306057
Digital data processing system.
Digitales Datenverarbeitungssystem.
Systeme de traitement de donnees numeriques.
PATENT ASSIGNEE:
DATA GENERAL CORPORATION, (410940), Route 9, Westboro Massachusetts 01581 , (US), (applicant designated states: AT;BE;CH;DE;FR;GB;IT;LI;LU;NL;SE)
INVENTOR:
Bachman, Brett L., 214 W. Canton Street Suite 4, Boston Massachusetts 02116, (US)
Bernstein, David H., 41 Bay Colony Drive, Ashland Massachusetts 01721, (US)
Bratt, Richard Glenn, 9 Brook Trail Road, Wayland Massachusetts 01778, (US)
Clancy, Gerald F., 13069 Jaccaranda Center, Saratoga California 95070, (US)
Gavrin, Edward S., Beaver Pond Road RFD 4, Lincoln Massachusetts 01773, (US)
Jones, Thomas M. Jones, 300 Reade Road, Chapel Hill North Carolina 27514, (US)
Katz, Lawrence H., 10943 S. Forest Ridge Road, Oregon City Oregon 97045, (US)
Mundie, Craig James, 136 Castlewood Drive, Cary North Carolina, (US)
Pilat, John F., 1308 Ravenhurst Drive, Raleigh North Carolina 27609, (US)
Schleimer, Stephen I., 1208 Ellen Place, Chapel Hill North Carolina 27514 , (US)
Wallach, Steven J., 12436 Green Meadow Lane, Saratoga California 95070, (US)
Wells, Douglas, M., 106 Robin Road, Chapel Hill North Carolina 27514, (US)
LEGAL REPRESENTATIVE:
Pears, David Ashley et al (34761), REDDIE & GROSE 16 Theobalds Road, London WC1X 8PL, (GB)
PATENT (CC, No, Kind, Date): EP 290110 A2 881109 (Basic)
EP 290110 A3 890412
APPLICATION (CC, No, Date): EP 88200916 820521;
PRIORITY (CC, No, Date): US 266401 810522
DESIGNATED STATES: AT; BE; CH; DE; FR; GB; IT; LI; LU; NL; SE
RELATED PARENT NUMBER(S) - PN (AN):
EP 67556
INTERNATIONAL PATENT CLASS (V7): G06F-012/06; G06F-009/30;
ABSTRACT WORD COUNT: 119
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text Language Update Word Count
CLAIMS A (English) EPABF1 1390
SPEC A (English) EPABF1 155314
Total word count - document A 156704
Total word count - document B 0
Total word count - documents A + B 156704

...SPECIFICATION s S-Interpreter Pointer (SIP) entry is a pointer, discussed in greater detail in a **following** discussion of CS 10110's microcode structure, pointing to the particular S-Interpeter (SINT) to...

...interpreting Procedure 11's SIN Code.
Referring finally to AIA 10352, AIA 10352 contains, as **previously** discussed, **information** pertaining to access rights required of any external procedure calling a 10318 procedure. There is...

12/3,K/8 (Item 8 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
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00270584
Full-duplex modem.
Vollduplex-Modem.
Modem full-duplex.
PATENT ASSIGNEE:
ADVANCED MICRO DEVICES, INC., (328120), 901 Thompson Place P.O. Box 3453, Sunnyvale, CA 94088, (US), (applicant designated states: AT;BE;CH;DE;ES;FR;GB;GR;IT;LI;LU;NL;SE)
INVENTOR:
Dunnion, Dermot, 3532 Geneva Drive, Santa Clara California 95051, (US)
LEGAL REPRESENTATIVE:
Wright, Hugh Ronald et al (38051), Brookes & Martin 52/54 High Holborn, London WC1V 6SE, (GB)
PATENT (CC, No, Kind, Date): EP 260889 A2 880323 (Basic)
EP 260889 A3 900207
EP 260889 B1 931020
APPLICATION (CC, No, Date): EP 87308048 870911;
PRIORITY (CC, No, Date): US 910111 860919
DESIGNATED STATES: AT; BE; CH; DE; ES; FR; GB; GR; IT; LI; LU; NL; SE
INTERNATIONAL PATENT CLASS (V7): H04L-005/14;
ABSTRACT WORD COUNT: 89

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text Language Update Word Count
CLAIMS B (English) EPBBF1 852
CLAIMS B (German) EPBBF1 756
CLAIMS B (French) EPBBF1 994
SPEC B (English) EPBBF1 1872
Total word count - document A 0
Total word count - document B 4474
Total word count - documents A + B 4474

...SPECIFICATION the receive-enable signal by the processor;
c) temporarily storing receive information in the receive **buffer memory** during a reception delay, wherein an amount of the receive information to be **stored** in the receive **buffer memory** corresponds to a difference between maximum and minimum values of the **variable** reception delay;
d) **interrupting** transmission of the **data** and initiating reception of the data **after** the variable reception **delay**, and

e) resuming **transmission** of the data when reception is completed.
The use an interrupt procedure in a modem...

12/3,K/9 (Item 9 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00201879
Multiple port integrated DMA and interrupt controller and arbitrator.
Mehrfachport-integrierter Steuerer und Arbitrierer fur DMA und Unterbrechungen.
Dispositif de commande et arbitre de DMA et d'interruptions integre a plusieurs portes.
PATENT ASSIGNEE:
International Business Machines Corporation, (200120), Old Orchard Road, Armonk, N.Y. 10504, (US), (applicant designated states: BE;CH;DE;FR;GB;IT;LI;NL;SE)
INVENTOR:
Burrus, Gilbert Steven, Jr., Turtle Creek No. 6, Rt. 5, Apex, NC 27502, (US)
Cooper, Ronald Julius, 6501 Wrenwood Ave., Raleigh, NC 27607, (US)
Marr, Michael Raymond, Rt. 5, Box 228A, Chapel Hill, NC 27514, (US)
Pescatore, John Carmine, 102 Valinda Dr., Chapel Hill, NC 27514, (US)
Marsico, Mario Anthony, 612 Crown Ct., Cary, NC 27511, (US)
LEGAL REPRESENTATIVE:
Lattard, Nicole (16571), Compagnie IBM France Departement de Propriete Intellectuelle, F-06610 La Gaude, (FR)
PATENT (CC, No, Kind, Date): EP 204960 A2 861217 (Basic)
EP 204960 A3 890816
EP 204960 B1 930804
APPLICATION (CC, No, Date): EP 86106185 860506;
PRIORITY (CC, No, Date): US 744852 850614
DESIGNATED STATES: BE; CH; DE; FR; GB; IT; LI; NL; SE
INTERNATIONAL PATENT CLASS (V7): G06F-013/34;
ABSTRACT WORD COUNT: 87

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text Language Update Word Count
CLAIMS B (English) EPBBF1 2349
CLAIMS B (German) EPBBF1 1099
CLAIMS B (French) EPBBF1 1338
SPEC B (English) EPBBF1 27770
Total word count - document A 0
Total word count - document B 32556
Total word count - documents A + B 32556

...SPECIFICATION a DMA receive request and it will activate a transmit DMA request when the transmit **buffer** is empty. DMA requests are handled by the DMA/interrupt controller and arbitrator (DIAC) as either DMA requests, interrupt requests or as both DMA and interrupt **requests**, depending upon how **the** program configures the DMA/interrupt controller and arbitrator (DIAC).

Thus, each communication port receive channel and transmit channel can **be** configured to operate using DMA **data transfers** or using

interrupt mode **transfers** to signal the processor to transfer another character or block of characters via **memory** mapped I/O command execution.

If a given channel is operated in a DMA mode...two common and distinct approaches for data service are the character driven interrupt method and **the** direct **memory** access method of data movement.

In the interrupt driven character service method, when a communications device, typically a USART, is ready to transmit or receive the data character, it **interrupts a** processor. The processor, **after** identifying the interrupting device through a unique interrupt vector presented by the device, usually enters an **interrupt service routine that** eventually causes it to execute the data transfer operation. It is usually desirable to transfer data to or from a **buffer** region in random access **memory** . Therefore, if the interrupting device is a receiver, the main processor will access its receive...

12/3,K/10 (Item 10 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00200280
Two-way ring communication system for elevator group control.
Zweirichtungsringverbindungssystem fur Aufzugsgruppensteuerung.
Systeme de communication en anneau a deux directions pour commande d'un groupe d'ascenseurs.
PATENT ASSIGNEE:
OTIS ELEVATOR COMPANY, (311771), 10 Farm Springs, Farmington, CT 06032, (US), (applicant designated states: AT;BE;CH;DE;FR;GB;IT;LI;LU;NL;SE)
INVENTOR:
Schlotter, Jurgen, Attendorner Weg 36, W-1000 Berlin 27, (DE)
Auer, Bruno, Soorstrasse 19, W-1000 Berlin 19, (DE)
LEGAL REPRESENTATIVE:
Henkel, Feiler, Hanzel & Partner (100401), Mohlstrasse 37, W-8000 Munchen 80, (DE)
PATENT (CC, No, Kind, Date): EP 239662 A1 871007 (Basic)
EP 239662 B1 930317
APPLICATION (CC, No, Date): EP 86104551 860403;
PRIORITY (CC, No, Date): EP 86104551 860403
DESIGNATED STATES: AT; BE; CH; DE; FR; GB; IT; LI; LU; NL; SE
INTERNATIONAL PATENT CLASS (V7): B66B-005/02; G05B-009/03; G06F-011/20;
ABSTRACT WORD COUNT: 219

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text Language Update Word Count
CLAIMS B (English) EPBBF1 220
CLAIMS B (German) EPBBF1 123
CLAIMS B (French) EPBBF1 140
SPEC B (English) EPBBF1 2982
Total word count - document A 0
Total word count - document B 3465
Total word count - documents A + B 3465

...SPECIFICATION Pool 120 which is the central function block, is a message buffer area used to **store** a number of messages until the messages are

processed.
Each message **stored** in the message pool is divided into three different fields. The first field 122 contains...

...by that message. The following four actions are required:
- Transmit message in left direction (to **previous** car controller).
- **Transmit message** in **right** direction (to **next** car controller).
- Process message if information determined for this car controller.
- Supervise and control the...

12/3,K/11 (Item 1 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00418748 **Image available**
SYSTEMS AND METHODS FOR SECURE TRANSACTION MANAGEMENT AND ELECTRONIC RIGHTS PROTECTION
SYSTEMES ET PROCEDES DE GESTION DE TRANSACTIONS SECURISEES ET DE PROTECTION DE DROITS ELECTRONIQUES
Patent Applicant/Assignee:
INTERTRUST TECHNOLOGIES CORP,
Inventor(s):
GINTER Karl L,
SHEAR Victor H,
SIBERT W Olin,
SPAHN Francis J,
VAN WIE David M,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9809209 A1 19980305
Application: WO 97US15243 19970829 (PCT/WO US9715243)
Priority Application: US 96706206 19960830
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH HU IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW GH KE LS MW SD SZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN ML MR NE SN TD TG
Publication Language: English
Fulltext Word Count: 195626

Fulltext Availability:
Detailed Description

Detailed Description
... such as consumers, business people, governments); and the privacy rights of parties described by electronic **information** , such as privacy rights related to information contained in a medical record, tax record, or...
?

NonPatent Literature Abstracts

File 8:Ei Compendex(R) 1884-2007/Jul W3
(c) 2007 Elsevier Eng. Info. Inc.
File 35:Dissertation Abs Online 1861-2007/Jul
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(c) 2007 NTIS, Intl Cpyrght All Rights Res
File 144:Pascal 1973-2007/Jul W3
(c) 2007 INIST/CNRS
File 34:SciSearch(R) Cited Ref Sci 1990-2007/Jul W5
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File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
(c) 2006 The Thomson Corp
File 99:Wilson Appl. Sci & Tech Abs 1983-2007/Jul
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File 266:FEDRIP 2007/Jul
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File 256:TecInfoSource 82-2007/Oct
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File 56:Computer and Information Systems Abstracts 1966-2007/Jul
(c) 2007 CSA.
File 60:ANTE: Abstracts in New Tech & Engineer 1966-2007/Jul
(c) 2007 CSA.

Set	Items	Description
S1	83466	MULTIPROCESSOR??? OR MULTI???()PROCESSOR???
S2	6247576	IMPORT?? OR IMPORTING OR EXPORT??? OR SEND??? OR TRANSFER? ? OR TRANSFERR??? OR COPY??? OR TRANSMIT? OR TRANSMISSION? ? - OR DISPATCH???
S3	35305	S2(3N)(SUSPEND? OR STALL??? OR DISCONTINU??? OR DELAY??? OR POSTPON??? OR DEFER??? OR INTERRUPT??? OR ABANDON?? OR HALT?-?? OR TERMINAT??? OR CEASE? ? OR CEASING OR DISRUPT???)
S4	14826945	DATA OR INFO OR INFORMATION OR MESSAGE? OR REPORT?
S5	42038	S4(3N)(SUSPEND? OR STALL??? OR DISCONTINU??? OR DELAY??? OR POSTPON??? OR DEFER??? OR INTERRUPT??? OR ABANDON?? OR HALT?-?? OR TERMINAT??? OR CEASE? ? OR CEASING OR DISRUPT???)
S6	2598105	BUFFER? OR CACHE? OR MEMORY OR STOR?
S7	1733	S5(5N)(PRIOR OR BEFORE???? OR PREVIOUS? OR PROCED??? OR IN-ITIAL? OR EARLY OR EARLIER)
S8	707	S3(5N)(AFTER???? OR LATER OR FOLLOW??? OR NEXT)
S9	0	S7 AND S8
S10	3420	S3 AND S5
S11	67	S10 AND S1
S12	52	RD (unique items)
S13	47	S12 NOT PY=2002:2007
S14	2867	S3(15N)S5

S15	65	S14 AND S1
S16	20	S14(25N)S1
S17	14	RD (unique items)
S18	11	S17 NOT PY=2002:2007
S19	0	S7(25N)S8(25N)S6
S20	265	S6 AND (S7 OR S8)
S21	126	S6(25N)(S7 OR S8)
S22	57	S6(5N)(S7 OR S8)
S23	0	S22 AND S1
S24	32	S22 NOT PY=2002:2007
S25	23	RD (unique items)
S26	23	S25 NOT S18

18/3,K/1 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

08687075 E.I. No: EIP00105378891
Title: Using duplication for the multiprocessor scheduling problem with hierarchical communications
Author: Bampis, Evripidis; Giroudeau, Rodolphe; Konig, Jean-Claude
Corporate Source: Universite d'Evry Val d'Essonne, Evry, Fr
Source: Parallel Processing Letters v 10 n 1 Mar 2000. p 133-140
Publication Year: 2000
CODEN: PPLTEE ISSN: 0219-6264
Language: English

...Abstract: case where all the tasks of the precedence graph have unit execution times, and the **multiprocessor** is composed by an unbounded number of clusters with two identical processors each. The communication **delay** for **transferring** the **data** between a predecessor-task and a successor-task executed on processors of different clusters take...

18/3,K/2 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

07383254 E.I. No: EIP96043143447
Title: Real-world testing ensures VMEbus reliability
Author: Wade, Dale; Durst, Jeff
Corporate Source: Heurikon Corp, Madison, WI, USA
Source: Electronic Design v 44 n 6 Mar 18 1996. 3pp
Publication Year: 1996
CODEN: ELODAW ISSN: 0013-4872
Language: English

...Abstract: that original VMEbus specification did not address some of the critical problems inherent in large **multiprocessor** systems. Perhaps the best way to ensure **multiprocessor** reliability is to test the board in a fully populated backplane with all boards performing arbitration, **interrupt**, **data transfer**, and read-modify-write transactions concurrently.

18/3,K/3 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04514409 E.I. Monthly No: EI8405040904 E.I. Yearly No: EI84025188
Title: POWERFUL VME BUS FEATURES EASE HIGH-LEVEL MU C APPLICATIONS.
Author: Hemenway, Jack E.
Corporate Source: Hemenway Corp, Boston, Mass, USA
Source: EDN v 29 n 1 Jan 12 1984 p 158-166, 168
Publication Year: 1984
CODEN: EDNSBH ISSN: 0012-7515
Language: ENGLISH

...Abstract: of chips, intended for industrial-control applications is considered for flexible data and address paths, **multiple processor0** support, nonmultiplexed and asynchronous **data transfers**, a powerful **interrupt** structure, or support for rapid failure detection. The standardization of the VME bus by IEEE...

18/3,K/4 (Item 4 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

03982683 E.I. Monthly No: EI8101002521 E.I. Yearly No: EI81028660
Title: FAST MULTIPROCESSOR REALIZATIONS OF DIGITAL FILTERS.
Author: Renfors, Markku; Neuvo, Yrjo
Corporate Source: Tampere Univ of Technol, Finl
Source: Rec IEEE Int Conf Acoust Speech Signal Process ICASSP 80, Proc, v 3, Denver, Colo, Apr 9-11 1980. Publ by IEEE (Cat n 80CH1559-4), Piscataway, NJ, 1980 p 916-919
Publication Year: 1980
CODEN: RIIPDR
Language: ENGLISH

...Abstract: period as a function of addition of multiplication times is introduced. Also the effect of **delays** in **data transfers** on the sampling period can be analyzed for different hardware configurations. Some examples are presented to show the use of the method in obtaining efficient **multiprocessor** realizations. 9 refs.

18/3,K/5 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

07455811 INSPEC Abstract Number: C2000-02-5440-016
Title: Choosing the number of processors in multiprocessor computing system
Author(s): Kovalenko, S.M.
Journal: Programmnye Produkty i Sistemy no.3 p.11-13
Publisher: Programmnye Produkty i Sistemy,
Publication Date: 1999 Country of Publication: Russia
CODEN: PPSTEF ISSN: 0236-235X
SICI: 0236-235X(1999)3L.11:CNPM;1-9
Material Identity Number: H078-1999-005
Language: Russian
Subfile: C

...Abstract: presented for the development of a methodology to estimate the number of processors in a **multiprocessor** computing system using as a criterion its maximum speed of response taking account of **delays** due to **data transfer** between processors.

18/3,K/6 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

05521790 INSPEC Abstract Number: C9312-4230M-016
Title: Retransmission control for communication on Hypertree multiprocessor systems
Author(s): Hirose, K.; Hama, H.
Author Affiliation: Fac. of Eng., Osaka City Univ., Japan
Journal: Memoirs of the Faculty of Engineering, Osaka City University vol.33 p.193-8
Publication Date: Dec. 1992 Country of Publication: Japan
CODEN: MFEOAR ISSN: 0078-6659
Language: English
Subfile: C

Abstract: In **multiprocessor** systems with message-passing architecture, the whole processing time is greatly influenced by the **message transmission delay** in communication. The authors propose a message retransmission control algorithm to reduce delay in communication...

18/3,K/7 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

03696884 INSPEC Abstract Number: C86041238
Title: Parallel implementation of the dynamic programming method
Author(s): Malinowski, K.; Sadecki, J.
Journal: Archiwum Automatyki i Telemechanika vol.30, no.3-4 p. 353-73
Publication Date: 1985 Country of Publication: Poland
CODEN: AATMAV ISSN: 0004-072X
Language: Polish
Subfile: C

...Abstract: facilities. The dynamic programming method possesses inherent features which allow for the efficient use of **multiprocessor** systems. Some parallel implementations of the dynamic programming method are presented. Since parallel algorithms may involve considerable overhead time due to **interrupts** handling and **data transfers**, it is essential to establish a realistic speed-up factor by taking into account this...

18/3,K/8 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal

13213504 PASCAL No.: 97-0480411
Stochastic model of a cache-coherency overhead in SCI rings
FIELD A J; HARRISON P G
Department of Computing. Imperial College, 180 Queen's Gate, London SW7 2BZ, United Kingdom
Journal: IEE proceedings. Computers and digital techniques, 1997, 144 (3) 175-186
Language: English

English Descriptors: Stochastic model; Shared memory; Interface; **Multiprocessor** ; Ring structure; Network architecture; Equilibrium state; **Message transmission** ; Markov process; **Delay** ; Single server queue

18/3,K/9 (Item 2 from file: 144)
DIALOG(R)File 144:Pascal

09191158 PASCAL No.: 90-0360340
Run-time scheduling and execution of loops on message passing machines
SALTZ J; CROWLEY K; RAVI MIRCHANDANEY; BERRYMAN H
NASA Langley res. cent., inst. computer applications sci. eng., Hampton VA 23065, USA
Journal: Journal of parallel and distributed computing, 1990, 8 (4) 303-312
Language: English

English Descriptors: Distributed system; Computer system; **Multiprocessor** ; **Message transmission** ; **Delay^Minimi zatio** ; Minimization; Program execution; Program loop; Integrated planning; Parallelization; Data dependency

18/3,K/10 (Item 3 from file: 144)
DIALOG(R)File 144:Pascal

08185027 PASCAL No.: 88-0185376
Simulating synchronous processors
WELCH J L
Journal: Information and computation, 1987, 74 (2) 159-171
Language: ENGLISH

English Descriptors: Distributed system; **Multiprocessor** ; Synchronous; Simulation; Modeling; **Message transmission** ; **Delay** time

18/3,K/11 (Item 1 from file: 95)
DIALOG(R)File 95:TEME-Technology & Management

00718712 I93092109259
Lower bounds and efficient algorithms for multiprocessor scheduling of directed acyclic graphs with communication delays
(Unter Schranken und effiziente Algorithmen fuer Mehrprozessorplanung von gerichteten azyklischen Graphen mit Kommunikationsverzoegerungen)
Jung, H; Kirousis, LM; Spirakis, P
Dept. of Math., Humboldt Univ., Berlin, Germany
Information and Computation, v105, n1, pp94-104, 1993
Document type: journal article Language: English
Record type: Abstract
ISSN: 0890-5401

...DESCRIPTORS: SCHEDULING; MULTIPROCESSING SYSTEMS; COMPUTER ARCHITECTURE; DATA COMMUNICATION; DATA NETWORK ADMINISTRATION; MASSIVELY PARALLEL

MACHINES; TREE STRUCTURE; **DELAY** TIME; **DATA TRANSMISSION** ; ALGORITHM THEORY; **MULTIPROCESSOR** INTERCONNECTION NETWORKS

26/3,K/1 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

08111077 E.I. No: EIP98094367536
Title: Step-down boosted-wordline scheme for 1-V battery-operated fast SRAM's
Author: Morimura, H.; Shibata, N.
Corporate Source: NTT Integrated Information & Energy Systems Lab, Atsugi-Shi, Jpn
Source: IEEE Journal of Solid-State Circuits v 33 n 8 Aug 1998. p 1220-1227
Publication Year: 1998
CODEN: IJSCBC ISSN: 0018-9200
Language: English

...Abstract: combined with current-sense amplifiers, is proposed. Boosting a selected-wordline voltage shortens the bitline **delay before** the **stored data** are sensed. The power dissipation while selecting a wordline is suppressed by stepping down the...

26/3,K/2 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

07145407 E.I. No: EIP95042678699
Title: Radix-2k Viterbi decoding with transpose path metric processor**
Author: Lee, Wen-Ta; Chen, Thou-Ho; Chen, Liang-Gee
Corporate Source: Natl Taiwan Univ, Taipei, Taiwan
Conference Title: Proceedings of the 1994 IEEE Asia-Pacific Conference on Circuits and Systems
Conference Location: Taipei, Taiwan Conference Date: 19941205-19941208
E.I. Conference No.: 42903
Source: IEEE Asia-Pacific Conference on Circuits and Systems - Proceedings 1994. IEEE, Piscataway, NJ, USA. p 194-199
Publication Year: 1994
CODEN: 002015
Language: English

...Abstract: simple local interconnection. For interconnection realization, the routing complexity is less than that of the **delay** -commutator **reported previously** . In addition, a higher **memory** length Viterbi processor can be constructed with lower radix-2**k modules. With features of...

26/3,K/3 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

07111885 E.I. No: EIP95032623940
Title: Two-stage vector quantization-lattice vector quantization

Author: Pan, Jianping; Fischer, Thomas R.
Corporate Source: Washington State Univ, Pullman, WA, USA
Source: IEEE Transactions on Information Theory v 41 n 1 Jan 1995. p 155-163
Publication Year: 1995
CODEN: IETTAW ISSN: 0018-9448
Language: English

...Abstract: 8 to 32, the signal-to-noise ratio performance is comparable or superior to equivalent- **delay** encoding results **previously reported** . For Gaussian sources with **memory** , the effectiveness of the encoding method is dependent on the feasibility of using a large...

26/3,K/4 (Item 4 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05225810 E.I. Monthly No: EIM8701-006562
Title: Implementation of a Powerful Local Area Network on a Fiber Optic Loop.
Title: IMPLEMENTATION EINES LEISTUNGSFAEHIGEN DATENNETZES MIT RINGSTRUKTUR AUF EINEM OPTISCHEN MEDIUM.
Author: Querasser, E.; Lindner, M.; Preineder, H.; Buschbeck, F.
Corporate Source: Austrian Research Cent Seibersdorf Ltd, Vienna, Austria
Conference Title: Real-Time Data Handling and Process Control - II: Real-Time Data Processing and Related Standards & Common Practices, Proceedings of the Second European Symposium.
Conference Location: Versailles, Fr Conference Date: 19821103
E.I. Conference No.: 08551
Source: Publ by North-Holland, Amsterdam, Neth and New York, NY, USA p 265-271
Publication Year: 1984
ISBN: 0-444-86846-1
Language: German

...Abstract: Seibersdorf. This future oriented implementation differs from other available local area networks especially in the **following** aspects: time-slotted system: defined **transmission delay** ; no **store** and forward; no local area network specific protocol; and optical medium in a loop configuration...

26/3,K/5 (Item 1 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01695258 ORDER NO: AAD99-22389
ALTERNATIVE STRATEGIES TO CONTROL SCALD OF APPLES AND SOME BIOCHEMICAL BASES (ALPHA FARNESENE, METHYL 5 HEPTENE 2 ONE, HYPOBARIC STORAGE)
Author: WANG, ZHENYONG
Degree: PH.D.
Year: 1998
Corporate Source/Institution: MICHIGAN STATE UNIVERSITY (0128)
Source: VOLUME 60/03-B OF DISSERTATION ABSTRACTS INTERNATIONAL.

PAGE 893. 160 PAGES

...hypobaric storage after one month delay in air. MHO in the epicuticular wax of fruits **stored** hypobarically **after** 2 or more months **delay** was released upon **transfer** of fruits to 20°C; MHO accumulated in direct proportion to the duration of...

26/3,K/6 (Item 2 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01679015 ORDER NO: AAD99-12644
RIO: A UNIVERSAL MULTIMEDIA STORAGE SYSTEM BASED ON RANDOM DATA ALLOCATION AND BLOCK REPLICATION (RANDOMIZED INPUT OUTPUT)
Author: SANTOS, JOSE RENATO GONCALVES
Degree: PH.D.
Year: 1998
Corporate Source/Institution: UNIVERSITY OF CALIFORNIA, LOS ANGELES (0031)
Source: VOLUME 59/11-B OF DISSERTATION ABSTRACTS INTERNATIONAL. PAGE 5942. 202 PAGES

...O) Multimedia Storage System which manages a set of parallel disks and supports real-time **data** retrieval with statistical **delay** guarantees. **Previous** work on multimedia **storage** systems has concentrated on video playback. RIO, however, is designed to support much more general...

26/3,K/7 (Item 3 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01427449 ORDER NO: AADAA-I9525329
VECTOR QUANTIZATION-LATTICE VECTOR QUANTIZATION AND ITS APPLICATIONS IN SPEECH CODING (CODEBOOK)
Author: PAN, JIANPING
Degree: PH.D.
Year: 1994
Corporate Source/Institution: WASHINGTON STATE UNIVERSITY (0251)
Source: VOLUME 56/04-B OF DISSERTATION ABSTRACTS INTERNATIONAL. PAGE 2226. 100 PAGES

...memoryless Gaussian and Laplacian sources, the signal-to-noise ratio performance is superior to equivalent- **delay** encoding results **previously reported** . For Gaussian sources with **memory** , the effectiveness of the encoding method is dependent on the feasibility of using a large...

26/3,K/8 (Item 4 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

904150 ORDER NO: AAD86-00713
PREDICTING ERRORS IN THE RECALL OF FIFTH- AND SIXTH-GRADERS: A STUDY IN INFERENTIAL RECONSTRUCTION (COMPREHENSION, MEMORY, SCHEMA, REMEMBERING)
Author: JOYNER, C. ROSANNE SOVINE
Degree: PH.D.
Year: 1985
Corporate Source/Institution: UNIVERSITY OF SOUTHERN MISSISSIPPI (0211)
Source: VOLUME 46/11-A OF DISSERTATION ABSTRACTS INTERNATIONAL. PAGE 3305. 101 PAGES

...was to determine if those students make errors of reconstruction due to the conditions of **story** ending, type of ancillary **information**, and/or **delay prior** to recall.
A total of 281 students was asked to read a story silently and...

...of story ending and delay prior to recall or by the three way interaction of **story** ending, ancillary **information**, and **delay prior** to recall.
The results of this study would suggest that fifth- and sixth-grade students...

26/3,K/9 (Item 5 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

841766 ORDER NO: AAD84-08790
ENHANCEMENT OF MEMORY IN THE MOUSE BY POST-TRAINING ADMINISTRATION OF ETHANOL
Author: COLBERN, DEBORAH LEE
Degree: PH.D.
Year: 1983
Corporate Source/Institution: UNIVERSITY OF CALIFORNIA, LOS ANGELES (0031)
Source: VOLUME 45/01-B OF DISSERTATION ABSTRACTS INTERNATIONAL. PAGE 394. 109 PAGES

...performance in any study described in this dissertation. This finding is sharply contrasted to the **memory disruption reported** when ethanol is given **prior** to training. Ethanol appears to be a non-specific modulator of ongoing events in the...

26/3,K/10 (Item 6 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

816601 ORDER NO: AAD83-15925
HIPPOCAMPAL OPIOID MECHANISMS OF MEMORY AND REWARD: THE GRANULE CELL MOSSY FIBER SYSTEM
Author: COLLIER, TIMOTHY JAMES
Degree: PH.D.

Year: 1983
Corporate Source/Institution: NORTHWESTERN UNIVERSITY (0163)
Source: VOLUME 44/03-B OF DISSERTATION ABSTRACTS INTERNATIONAL. PAGE 950. 129 PAGES

...aspects of the maze task or for the inhibitory avoidance task. Granule cell stimulation delivered **before** the learning trial did not **disrupt** registration of **information** into declarative **memory**.

Consistent with anatomical evidence that the granule cells contain opioid peptides, the declarative memory-specific...

26/3,K/11 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

07460557 INSPEC Abstract Number: B2000-02-6150M-081
Title: Effect of channel memory on retransmission protocols for low energy wireless data communications
Author(s): Choi, J.D.; Wasserman, K.M.; Stark, W.E.
Author Affiliation: Dept. of Electr. Eng. & Comput. Sci., Michigan Univ., Ann Arbor, MI, USA
Conference Title: 1999 IEEE International Conference on Communications (Cat. No. 99CH36311) Part vol.3 p.1552-6 vol.3
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 1999 Country of Publication: USA 3 vol (xl+2061) pp.
ISBN: 0 7803 5284 X Material Identity Number: XX-1999-02122
U.S. Copyright Clearance Center Code: 0 7803 5284 X/99/$10.00
Conference Title: 1999 IEEE International Conference on Communications
Conference Sponsor: AG Communication Systems; Lucent Technologies; Transwitch; Nortel Networks; Sierra Wireless; BCTEL; IBM; Ericsson
Conference Date: 6-10 June 1999 Conference Location: Vancouver, BC, Canada
Language: English
Subfile: B

...Abstract: that the protocol always favors attempting transmissions when the memory is low. As the channel **memory** increases, the protocol **suspends transmission** for longer durations **after** a packet failure.

26/3,K/12 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

06152774 INSPEC Abstract Number: B9602-6120B-032
Title: The radix-2/sup k/ Viterbi decoding with transpose path metric processor
Author(s): Wen-Ta Lee; Thou-Ho Chen; Liang-Gee Chen
Author Affiliation: Dept. of Electr. Eng., Nat. Taiwan Univ., Taipei, Taiwan
Conference Title: APCCAS `94. 1994 IEEE Asia-Pacific Conference on Circuits and Systems (Cat. No.94TH8029) p.194-9
Publisher: IEEE, New York, NY, USA
Publication Date: 1994 Country of Publication: USA xv+684 pp.

ISBN: 0 7803 2440 4 Material Identity Number: XX94-00164
U.S. Copyright Clearance Center Code: 0 7803 2440 4/94/$4.00
Conference Title: Proceedings of APCCAS'94 - 1994 Asia Pacific Conference on Circuits and Systems
Conference Sponsor: IEEE CAS Soc.; IEEE CAS Taipei Chapter; IEEE Taipei Sect.; IEEE Signal Process. Soc.; Nat. Sci. Council; Minstr. Educ.; Nat. Chiao Tung Univ.; Nat. Tsing Hua Univ.; Nat. Taiwan Univ.; Nat. Central Univ.; Nat. Chung Cheng Univ.; Inst. Inf. Ind.; Ind. Technol. Res. Inst.; Chung Shan Inst. Sci. & Technol.; Ministry of Transp. & Commun.; MOTC; Nat. Sci. Council Local Ind
Conference Date: 5-8 Dec. 1994 Conference Location: Taipei, Taiwan
Language: English
Subfile: B

...Abstract: simple local interconnection. For interconnection realization, the routing complexity is less than that of the **delay** -commutator **reported previously** . In addition, a higher **memory** length Viterbi processor can be constructed with lower radix-2/sup k/ modules. With features...

26/3,K/13 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

05893665 INSPEC Abstract Number: B9504-6120B-074
Title: Two-stage vector quantization-lattice vector quantization
Author(s): Jianping Pan; Fischer, T.R.
Author Affiliation: Dept. of Electr. Eng. & Comput. Sci., Washington State Univ., Pullman, WA, USA
Journal: IEEE Transactions on Information Theory vol.41, no.1 p. 155-63
Publication Date: Jan. 1995 Country of Publication: USA
CODEN: IETTAW ISSN: 0018-9448
U.S. Copyright Clearance Center Code: 0018-9448/95/$04.00
Language: English
Subfile: B

...Abstract: 8 to 35 the signal-to-noise ratio performance is comparable or superior to equivalent- **delay** encoding results **previously reported** . For Gaussian sources with **memory** , the effectiveness of the encoding method is dependent on the feasibility of using a large...

26/3,K/14 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

03220310 INSPEC Abstract Number: C84017731
Title: Bullet-proof Pascal input
Author(s): Hinnant, D.F.; Smith, M.B.
Journal: BYTE vol.9, no.2 p.428-34
Publication Date: Feb. 1984 Country of Publication: USA
CODEN: BYTEDJ ISSN: 0360-5280

Language: English
Subfile: C

...Abstract: reinitialise; data can be lost or corrupted when disc files are not properly closed or **buffers** are not flushed **before** program **termination** . The **data** -input error problem surfaces when data of an unexpected type is entered. This is most...

26/3,K/15 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

01024360 INSPEC Abstract Number: C69003774
Title: Communication control program (check off method)
Author(s): Ohigashi, H.; Kawai, H.; Sato, M.; Wanabe, T.
Journal: Bulletin of the Electrotechnical Laboratory vol.32, no.8 p.826-38
Publication Date: 1968 Country of Publication: Japan
CODEN: DESIA7 ISSN: 0366-9092
Language: Japanese
Subfile: C

...Abstract: interface software module. Functions of subroutines of the CCP are explained. The subroutines are the **Initializer** , the **Interruption** Analyzer, the **Data** Typewriter Manager (DTM) the **Buffer** Control, the Line Program, the Entrance, and the Reporter. The independent process 'CLOCK' /sub /actuated...

26/3,K/16 (Item 1 from file: 6)
DIALOG(R)File 6:NTIS

1840967 NTIS Accession Number: AD-A285 153/3
Calcasieu River Sediment Removal Study
(Final rept)
Wade, R.
Army Engineer Waterways Experiment Station, Vicksburg, MS. Environmental Lab.
Corp. Source Codes: 002621009; 411388
Report No.: WES/TR/EL-94-9
Aug 94 97p
Languages: English
Journal Announcement: GRAI9502
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A05/MF A02

... dredged and placed in a CDF. The compression tests data were used to develop the **initial storage** requirements. The flocculent tests **data** indicated that the **suspended** solids will settle by gravity. Results of the modified elutriate tests, which predict both dissolved...

26/3,K/17 (Item 2 from file: 6)
DIALOG(R)File 6:NTIS

0566711 NTIS Accession Number: HRP-0007470/8/XAB
Multidimensional Problem-Oriented Review and Evaluation System
Miller, S. I. ; Schlachter, R. H.
Case Western Reserve Univ., Cleveland, Ohio. School of Medicine.
1974 4p
Document Type: Journal article
Journal Announcement: GRAI7621
Pub. in the American Jnl. of Psychiatry, v132 n3 p232-235 Mar 75.
NTIS Prices: Not available NTIS

... time treatment is terminated, and includes information about the treatment and its outcome. Both the **initial** evaluation **information** and the **termination** outcome **information** are **stored** on computer discs. The system provides two different types of output: a monthly summary of...

26/3,K/18 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal

14849367 PASCAL No.: 00-0534058
Hypobaric storage removes scald-related volatiles during the low temperature induction of superficial scald of apples
ZHENYONG WANG; DILLEY David R
Department of Horticulture, Michigan State University, East Lansing, MI 48824, United States
Journal: Postharvest biology and technology, 2000, 18 (3) 191-199
Language: English

... or more delay in air. MHO which had partitioned in the epicuticular wax of fruit **stored** hypobarically **after** 2 or more months **delay** was released upon **transfer** of fruit to atmospheric pressure of 20 Degree C; MHO accumulated and/or was produced...

26/3,K/19 (Item 2 from file: 144)
DIALOG(R)File 144:Pascal

14598180 PASCAL No.: 00-0266277
Concurrent modulation of anxiety and memory
WALL P M; MESSIER C
School of Psychology, University of Ottawa, Vanier: Room 215, Ottawa, Ont., K1N 6N5, Canada
Journal: Behavioural brain research, 2000, 109 (2) 229-241
Language: English

... transfer-latencies and produced an anxiogenic behavioural profile in the first elevated plus-maze trial. **Following** a 24 h **delay**, **transfer** -latency reference **memory** was not influenced, but a robust anxiogenic behavioural profile was observed in the second no...

26/3,K/20 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

08553268 Genuine Article#: 299RF No. References: 33
Title: Hypobaric storage removes scald-related volatiles during the low temperature induction of superficial scald of apples
Author(s): Wang ZY; Dilley DR (REPRINT)
Corporate Source: MICHIGAN STATE UNIV,DEPT HORT/E LANSING//MI/48824 (REPRINT); MICHIGAN STATE UNIV,DEPT HORT/E LANSING//MI/48824
Journal: POSTHARVEST BIOLOGY AND TECHNOLOGY, 2000, V18, N3 (APR), P191-199
ISSN: 0925-5214 Publication date: 20000400
Publisher: ELSEVIER SCIENCE BV, PO BOX 211, 1000 AE AMSTERDAM, NETHERLANDS
Language: English Document Type: ARTICLE (ABSTRACT AVAILABLE)

...Abstract: or more delay in air. MHO which had partitioned in the epicuticular wax of fruit **stored** hypobarically **after** 2 or more months **delay** was released upon **transfer** of fruit to atmospheric pressure of 20 degrees C; MHO accumulated and/or was produced...

26/3,K/21 (Item 2 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

06950000 Genuine Article#: 106RY No. References: 40
Title: Peptidyl-prolyl-cis/trans-isomerase activity may be necessary for memory formation
Author(s): Bennett PC; Singaretnam LG; Zhao WQ; Lawen A (REPRINT) ; Ng KT
Corporate Source: MONASH UNIV,DEPT BIOCHEM & MOL BIOL, WELLINGTON RD/CLAYTON/VIC 3168/AUSTRALIA/ (REPRINT); MONASH UNIV,DEPT BIOCHEM & MOL BIOL/CLAYTON/VIC 3168/AUSTRALIA/; MONASH UNIV,DEPT PSYCHOL/CLAYTON/VIC 3168/AUSTRALIA/
Journal: FEBS LETTERS, 1998, V431, N3 (JUL 24), P386-390
ISSN: 0014-5793 Publication date: 19980724
Publisher: ELSEVIER SCIENCE BV, PO BOX 211, 1000 AE AMSTERDAM, NETHERLANDS
Language: English Document Type: ARTICLE (ABSTRACT AVAILABLE)

...Abstract: cis/transisomerases (PPIases, EC 5.2.1.8) is emerging, Cyclosporin A (CyA) has been **previously reported** to **disrupt memory** formation in a temporally specific manner, when administered intracranially to day-old chicks trained on...

26/3,K/22 (Item 3 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

04706706 Genuine Article#: UC121 No. References: 31
Title: PREFRONTAL CORTEX AND WORKING-MEMORY FOR SPATIAL RESPONSE,

SPATIAL
LOCATION, AND VISUAL OBJECT INFORMATION IN THE RAT
Author(s): KESNER RP; HUNT ME; WILLIAMS JM; LONG JM
Corporate Source: UNIV UTAH,DEPT PSYCHOL/SALT LAKE CITY//UT/84112
Journal: CEREBRAL CORTEX, 1996, V6, N2 (MAR-APR), P311-318
ISSN: 1047-3211
Language: ENGLISH Document Type: ARTICLE (Abstract Available)

...Abstract: even at the shortest delay In the second experiment, rats were trained on a working **memory** task for spatial location **information** using a **delayed** matching-to-sample **procedure** . Following lesions of the MPF. there was only a mild working memory deficit, whereas following...

...even at the shortest delay. In the third experiment, rats were trained on a working **memory** task for visual object **information** using a **delayed** nonmatching-to-sample **procedure** . Following lesions of the MPF, there were no working memory deficits, whereas following lesions of...

26/3,K/23 (Item 1 from file: 56)
DIALOG(R)File 56:Computer and Information Systems Abstracts

0000255076 IP ACCESSION NO: 0170376
Radix-2 super(k) Viterbi decoding with transpose path metric processor

Lee, Wen-Ta; Chen, Thou-Ho; Chen, Liang-Gee
Natl Taiwan Univ, Taipei, Taiwan

PAGES: 194-199
PUBLICATION DATE: 1994

PUBLISHER: IEEE, PISCATAWAY, NJ, (USA)

CONFERENCE:
The 1994 IEEE Asia-Pacific Conference on Circuits and Systems, Taipei, Taiwan, 05-08 Dec. 1994

DOCUMENT TYPE: Conference Paper
RECORD TYPE: Abstract
LANGUAGE: English
FILE SEGMENT: Computer & Information Systems Abstracts

ABSTRACT:
... simple local interconnection. For interconnection realization, the routing complexity is less than that of the **delay** -commutator **reported previously** . In addition, a higher **memory** length Viterbi processor can be constructed with lower radix-2 super(k) modules. With features...
?

NonPatent Literature Fulltext

File 275:Gale Group Computer DB(TM) 1983-2007/Jul 24
(c) 2007 The Gale Group
File 47:Gale Group Magazine DB(TM) 1959-2007/Jul 19
(c) 2007 The Gale group
File 621:Gale Group New Prod.Annou.(R) 1985-2007/Jul 30
(c) 2007 The Gale Group
File 636:Gale Group Newsletter DB(TM) 1987-2007/Aug 02
(c) 2007 The Gale Group
File 148:Gale Group Trade & Industry DB 1976-2007/Jul 31
(c)2007 The Gale Group
File 624:McGraw-Hill Publications 1985-2007/Aug 02
(c) 2007 McGraw-Hill Co. Inc
File 98:General Sci Abs 1984-2007/Jul
(c) 2007 The HW Wilson Co.
File 553:Wilson Bus. Abs. 1982-2007/Aug
(c) 2007 The HW Wilson Co
File 15:ABI/Inform(R) 1971-2007/Aug 02
(c) 2007 ProQuest Info&Learning
File 635:Business Dateline(R) 1985-2007/Aug 02
(c) 2007 ProQuest Info&Learning
File 9:Business & Industry(R) Jul/1994-2007/Jul 30
(c) 2007 The Gale Group
File 610:Business Wire 1999-2007/Aug 03
(c) 2007 Business Wire.
File 810:Business Wire 1986-1999/Feb 28
(c) 1999 Business Wire
File 647:CMP Computer Fulltext 1988-2007/Sep W2
(c) 2007 CMP Media, LLC
File 674:Computer News Fulltext 1989-2006/Sep W1
(c) 2006 IDG Communications
File 369:New Scientist 1994-2007/Jul W2
(c) 2007 Reed Business Information Ltd.
File 613:PR Newswire 1999-2007/Aug 03
(c) 2007 PR Newswire Association Inc
File 813:PR Newswire 1987-1999/Apr 30
(c) 1999 PR Newswire Association Inc
File 370:Science 1996-1999/Jul W3
(c) 1999 AAAS
File 16:Gale Group PROMT(R) 1990-2007/Aug 02
(c) 2007 The Gale Group
File 160:Gale Group PROMT(R) 1972-1989
(c) 1999 The Gale Group
File 484:Periodical Abs Plustext 1986-2007/Jul W5
(c) 2007 ProQuest
File 634:San Jose Mercury Jun 1985-2007/Aug 02
(c) 2007 San Jose Mercury News
File 696:DIALOG Telecom. Newsletters 1995-2007/Aug 02
(c) 2007 Dialog

Set Items Description
S1 67817 MULTIPROCESSOR??? OR MULTI???()PROCESSOR???
S2 10315229 IMPORT?? OR IMPORTING OR EXPORT??? OR SEND??? OR TRANSFER?
? OR TRANSFERR??? OR COPY??? OR TRANSMIT? OR TRANSMISSION? ? -

OR DISPATCH???
S3 68693 S2(3N)(SUSPEND? OR STALL??? OR DISCONTINU??? OR DELAY??? OR POSTPON??? OR DEFER??? OR INTERRUPT??? OR ABANDON?? OR HALT?-?? OR TERMINAT??? OR CEASE? ? OR CEASING OR DISRUPT???)
S4 36246387 DATA OR INFO OR INFORMATION OR MESSAGE? OR REPORT?
S5 147761 S4(3N)(SUSPEND? OR STALL??? OR DISCONTINU??? OR DELAY??? OR POSTPON??? OR DEFER??? OR INTERRUPT??? OR ABANDON?? OR HALT?-?? OR TERMINAT??? OR CEASE? ? OR CEASING OR DISRUPT???)
S6 10869203 BUFFER? OR CACHE? OR MEMORY OR STOR?
S7 8041 S5(5N)(PRIOR OR BEFORE???? OR PREVIOUS? OR PROCED??? OR INITIAL? OR EARLY OR EARLIER)
S8 2886 S3(5N)(AFTER???? OR LATER OR FOLLOW??? OR NEXT)
S9 0 S1(25N)S7(25N)S8
S10 0 S1(100N)S7(100N)S8
S11 1 S7(25N)S8
S12 3792 S3(25N)S5
S13 6 S12(25N)S1
S14 18 S1(100N)S12
S15 16 RD (unique items)
S16 16 S15 NOT S11
S17 15 S16 NOT PY=2002:2007

11/3,K/1 (Item 1 from file: 624)
DIALOG(R)File 624:McGraw-Hill Publications

0137670
CANOLIMON DELAYED ADDITIONALLY
Platts Oilgram Price Report, Vol. 67, No. 130, Pg 1-A
July 10, 1989
JOURNAL CODE: POP
SECTION HEADING: MARKET NEWS & NOTES ISSN: 0162-1292
WORD COUNT: 277

TEXT:

... by Colombian rebels will delay resumption of Canolimon exports to mid-July, sources at Ecopetrol **report** . **Exports** have been **halted** since June 16 **following earlier** bombings. That estimate of a resumption in liftings appears substantiated by news of a Canolimon...

17/3,K/1 (Item 1 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01697096 SUPPLIER NUMBER: 15694397 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Future PC designs demand high-speed I/Os, fast graphics, and low power.
Bursky, Dave
Electronic Design, v42, n14, p38(2)
July 11, 1994
ISSN: 0013-4872 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 1405 LINE COUNT: 00116

... graphics subsystems also will be spotlighted. Papers in various sessions will cover such issues as **multiprocessor** system design, designing with x86 and Power PC microprocessors, the optimization of clocking and skew...

...will impact the way graphics memory subsystems will have to be designed to ensure low- **delay data transfers** . I/O buses such as the 100-Mbit/s (extendible to 400 Mbits/s) P1394...

17/3,K/2 (Item 2 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01507159 SUPPLIER NUMBER: 12015412 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Interface chips applied to multiprocessing architectures.
James, Jeremy
Computer Design, v31, n2, p82(1)
Feb, 1992
ISSN: 0010-4566 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 949 LINE COUNT: 00083

... of this, there are many successful and sophisticated VMEbus systems.

The additional flexibility of a **multiprocessor** architecture requires that the system designer make more major decisions regarding the system design including...

...The VMEbus standard provides enough information for a vendor to design an interface including arbitration, **interrupting** and **data transfer**. **Multiprocessor** systems, however, communicate at a higher level and the system designer will want to define...

...compliant with the VMEbus spec.

The last two advantages are not as evident. Presumably the **multiprocessor** application will be a concurrent program consisting of several tasks configured via some mechanism to...

17/3,K/3 (Item 3 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01426055 SUPPLIER NUMBER: 10487888 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Multiprocessing on high-end bus architectures. (includes related article on efficient use of bus bandwidth; part 9 of Bus Compatible Board Series)
Peckham, Clarence
I&CS (Instrumentation & Control Systems), v64, n1, p57(4)
Jan, 1991
ISSN: 0746-2395 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 2101 LINE COUNT: 00172

TEXT:

Multiprocessing on high-end bus architectures In selecting a standard bus architecture for a distributed **multiprocessor** system, designers must evaluate a wide range of capabilities. Because **multiprocessor** system architectures are so diverse, hardware protocols and mechanisms specific to multiprocessing are typically not...

...still gain insight into the multiprocessing capabilities of each bus by evaluating their protocols for **data transfer**, arbitration, **interrupt** handling, and cache control.

17/3,K/4 (Item 4 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01383288 SUPPLIER NUMBER: 09482253 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Embedded PCs: design the application, not the computer. (Bus Compatible Board Series, part 7c)
Cooper, Steve
I&CS (Instrumentation & Control Systems), v63, n9, p77(4)
Sept, 1990
ISSN: 0746-2395 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 2718 LINE COUNT: 00212

... bus. Interfacing software consists of three types: bus access software, standard I/O drivers, and **multiprocessor** interfacing software.

Bus access software consists of a library of prewritten routines that can be liked to an application for easily callable bus interfacing. There routines include **send interrupt**, set **interrupt** handler address, wait for **interrupt**, write block of **data**, read block of data, etc. The bus access library takes away any need for the...

17/3,K/5 (Item 1 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

08656716 SUPPLIER NUMBER: 18254431 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Real-world testing ensures VMEbus reliability.(Engineering Software)
Wade, Dale; Durst, Jeff
Electronic Design, v44, n6, p136(3)
March 18, 1996
ISSN: 0013-4872 LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 2292 LINE COUNT: 00187

...ABSTRACT: problems by adopting real-world testing. Boards should be tested extensively in a real-world **multiprocessor** system environment immediately after they are manufactured and before they are released to the customer...

...approach using a three-week test suite called the Gauntlet, which verifies system-level arbitration, **interrupt**, **data transfer** and read-modify-write functions in a 21-slot VMEbus enclosure.

... But these guidelines address only a fraction of the design issues that are critical for **multiprocessor** systems.

To ensure that CPU boards work reliably in a **multiprocessor** environment, board manufacturers and system integrators should institute test procedures that exhaustively exercise the boards...

...verify on-card functionality and bus transactions are inadequate. The only way to effectively validate **multiprocessor** reliability is to test the board in a fully populated backplane with all boards performing arbitration, **interrupt**, **data transfer**, and read-modify-write transactions concurrently.

VMEBUS GOTCHAS

Perhaps the most significant cause of reliability...

...that board designers can increase the likelihood that their boards will perform reliably in a **multi**processor system is to simulate the design extensively. Through simulation, designers can spot and correct marginal...

...Once a board has been manufactured, it should be tested extensively in a real-world **multiprocessor** system environment before release to the customer. At Heurikon, every CPU board must survive an...

...week test suite known as the Gauntlet, which verifies the board's system-level arbitration, **data transfer**, **interrupt**, and read-modify-write capabilities in a fully populated, fully loaded, 21-slot VME-bus enclosure. The Gauntlet is also used to verify VSB (VME subsystem bus) **multiprocessor** functionality and reliability.

Before stepping up to the rigors of the Gauntlet, Heurikon's boards...

17/3,K/6 (Item 2 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2007 The Gale Group. All rts. reserv.

08611906 SUPPLIER NUMBER: 18211102 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Multiprocessing demands.(EE Times Supplement on VME) (Technology Information)
Wade, Dale
Electronic Engineering Times, n897, pV8(1)
April 15, 1996
ISSN: 0192-1541 LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 901 LINE COUNT: 00076

... transactions between a pair of boards. What's needed is an exhaustive suite of arbitration, **interrupt** , **data - transfer** and read-modify-write tests that are performed concurrently in a fully populated backplane.
Capacitive...

...sensitive to faulty signal oscillations and other glitches.
Another potential source of reliability problems in **multiprocessor** systems is signal coupling between data and control lines. Because of the physical proximity of...

17/3,K/7 (Item 3 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2007 The Gale Group. All rts. reserv.

03882606 SUPPLIER NUMBER: 07111876 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Bus-analysis tools isolate tough problems. (technical)
Leibson, Steven H.
EDN, v34, n3, p91(7)
Feb 2, 1989
DOCUMENT TYPE: technical ISSN: 0012-7515 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 1930 LINE COUNT: 00150

... Beyond bus analysis
Complex buses such as the VME Bus support transactions other than simple **data transfers** and **interrupts** . The VME Bus accommodates distributed interrupt handlers and multiple bus masters. These VME Bus features allow you to create complex, **multiprocessor** systems that are often tough to debug. If you should encounter problems with such a...

17/3,K/8 (Item 1 from file: 810)
DIALOG(R)File 810:Business Wire
(c) 1999 Business Wire . All rts. reserv.

0396047 BW827

MAGNALINK: Magnalink Communications To Provide Leading WAN Data Compression Technology To Computer Network Technology Corporation Under OEM

Agreement

April 5, 1994

Byline: Business Editors

...speeds,
resulting in faster network response times, higher data integrity, less network congestion, and fewer **data transmission delays**. Increased throughput also reduces bandwidth requirements and yields significant cost savings by eliminating the need...

...optimal WAN capacity and performance while reducing their network costs."

Featuring an advanced pipeline and **multiprocessor** architecture, Magnalink's WAN data compression technology delivers up to 4:1 data compression ratios...

17/3,K/9 (Item 1 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext

01087818 CMP ACCESSION NUMBER: EET19960415S0006
Multiprocessing demands
Dale Wade
ELECTRONIC ENGINEERING TIMES, 1996, n 897, PGV8
PUBLICATION DATE: 960415
JOURNAL CODE: EET LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: VME Takes Center Stage - A Supplement To EET
WORD COUNT: 843

... transactions between a pair of boards. What's needed is an exhaustive suite of arbitration, **interrupt**, **data - transfer** and read-modify-write tests that are performed concurrently in a fully populated backplane.

Capacitive...

...sensitive to faulty signal oscillations and other glitches.

Another potential source of reliability problems in **multiprocessor** systems is signal coupling between data and control lines. Because of the physical proximity of...

17/3,K/10 (Item 2 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext

01014941 CMP ACCESSION NUMBER: EET19940718S0208
On-chip multiprocessing melds DSPs
ELECTRONIC ENGINEERING TIMES, 1994, n 806, 55
PUBLICATION DATE: 940718
JOURNAL CODE: EET LANGUAGE: English
RECORD TYPE: Fulltext
WORD COUNT: 1967

... most powerful DSPs or general-purpose processors previously available.

Application distribution

The main differences between **multiprocessor** and single-DSP implementations lie in distributing the application across the processors. Unless carefully designed, the effects of combining **multiple processors** in a system can negate any performance gains expected in the aggregate system. A parallel...

...Such mechanisms can interfere with software execution speed.

For example, inefficiencies can arise when communication **messages**, or other event **interrupts** between processors, occur in an asynchronous fashion, introducing **delays** on either the **sending** or receiving processor(s). The performance impact due to such random interprocessor events can be...

17/3,K/11 (Item 3 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext

00552421 CMP ACCESSION NUMBER: CRN19930111S10808
Heurikon targetsboard at OEMs
COMPUTER RESELLER NEWS, 1993, n 507, 137
PUBLICATION DATE: 930111
JOURNAL CODE: CRN LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: sourcing
WORD COUNT: 400

... co-processor.

To verify the board's appropriateness for multiprocessing applications, Heurikon developed the Gauntlet **multiprocessor** test suite. It combines a sequence of arbitration, **data transfer**, **interrupt** and I/O tests.

Executed in a fully loaded, fully populated VMEbus enclosure (21 boards...

17/3,K/12 (Item 1 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

04300797 Supplier Number: 46303648 (USE FORMAT 7 FOR FULLTEXT)
Multiprocessing demands
Electronic Engineering Times, pV8
April 15, 1996
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 837

... transactions between a pair of boards. What's needed is an exhaustive suite of arbitration, **interrupt**, **data - transfer** and read-modify-write tests that are performed concurrently in a fully populated backplane.

Capacitive...

...sensitive to faulty signal oscillations and other glitches.
Another potential source of reliability problems in **multiprocessor** systems is signal coupling between data and control lines. Because of the physical proximity of...

17/3,K/13 (Item 2 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

03470695 Supplier Number: 44846706 (USE FORMAT 7 FOR FULLTEXT)
On-chip multiprocessing melds DSPs
Electronic Engineering Times, p55
July 18, 1994
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 1938

... most powerful DSPs or general -purpose processors previously available.
Application distribution
The main differences between **multiprocessor** and single-DSP implementations lie in distributing the application across the processors. Unless carefully designed, the effects of combining **multiple processors** in a system can negate any performance gains expected in the aggregate system. A parallel...

...Such mechanisms can interfere with software execution speed.
For example, inefficiencies can arise when communication **messages**, or other event **interrupts** between processors, occur in an asynchronous fashion, introducing **delays** on either the **sending** or receiving processor(s). The performance impact due to such random interprocessor events can be...

17/3,K/14 (Item 3 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

03221921 Supplier Number: 44421362 (USE FORMAT 7 FOR FULLTEXT)
Sky boosts VME limit
Electronic Engineering Times, p62
Feb 7, 1994
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 661

... the blocking that normally occurs while the bus is servicing read or write requests from **multiple processors**. It sends data in packets between FIFOs, at each interface utilizing separate hardware arbitration. Once...

...Hardware arbitration frees the bus to directly blast data between interfaces. In traditional VME architectures **data transfers** are

delayed while a path is established between processors. The result is increased latency and blocking.

To...

17/3,K/15 (Item 4 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

02678579 Supplier Number: 43573832 (USE FORMAT 7 FOR FULLTEXT)
Heurikon targets board at OEMs
Computer Reseller News, p137
Jan 11, 1993
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 403

... co-processor.

To verify the board's appropriateness for multiprocessing applications, Heurikon developed the Gauntlet **multiprocessor** test suite. It combines a sequence of arbitration, **data transfer**, **interrupt** and I/O tests.

Executed in a fully loaded, fully populated VMEbus enclosure (21 boards...